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ADAPTIVE CONTROL SYSTEM
VOLUME I - EQUIPMENT AND TESTING



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DRF, INC.
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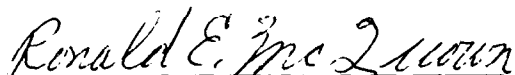
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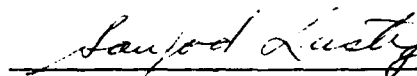
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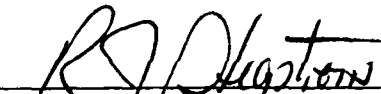


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SUMMARY

The contract was performed for the Experimental Control Group, Structures Test Branch, Department of the Air Force and was supervised by Mr. Ronald E. McQuown. The capabilities of the electronic controllers to establish the desired level of dynamic response in the electro-hydraulic loading systems was greatly improved by the addition of resonance compensation, integral compensation, and feedforward networks. Precise adjustment of the control system was aided by computer control of the networks and a computer based frequency response analyzer. Three complete channels of the control hardware and one frequency response analyzer were manufactured and delivered. These items were all proven in field testing under actual conditions used in the Structures Laboratory at WPAFB. Software was developed to run the frequency response analyzer, to optimize the adjustments of the compensation system and to set the reset and gain of the controller boards also provided with the system, and to operate the frequency response hardware in a second mode wherein they gather and analyze on-line data of the control system performance. It was clearly demonstrated that this approach for upgrading the electronic controllers and using the computer along with the frequency response measuring equipments, resulted in greatly improved dynamic response permitting more rapid system setup and faster running of the programs used in fatigue test work.

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FOREWORD

This final report describes technical work accomplished during the Adaptive Control System program conducted under Contract F33615-83-C-3203. The work described was performed during the period May 1983 - March 1985. This contract with DRF, Inc. was sponsored by the Flight Dynamics Laboratory, WPAFB, OH, with Mr. Ronald M. McQuown (AFWAL/FIBTC) as project engineer.

The report was submitted by the author, Mr. Abraham M. Fuchs, in September 1985.

TABLE OF CONTENTS

<u>SECTION</u>		<u>PAGE</u>
1	INTRODUCTION	1
	1.1 GENERAL	1
	1.2 THE CONTROLLER	2
	1.3 FREQUENCY RESPONSE MEASUREMENT	3
	1.4 DIGITAL DATA TAKING	4
	1.5 OVERALL REPORT ORGANIZATION	5
2	FREQUENCY RESPONSE MEASUREMENT	7
	2.1 BASICS	7
	2.2 TEST SIGNAL GENERATOR	8
	2.2.1 Frequency and Waveshape	8
	2.2.2 Output Amplitude and DC Offset	9
	2.2.3 Mechanical	10
	2.3 INPUT AMPLIFIER AND ALIAS FILTER (TWO CHANNELS)	11
	2.3.1 General	11
	2.3.2 Input Amplifier - Gain Setting	11
	2.3.3 Input Amplifier - DC Reject Circuit	12
	2.3.4 Alias Filter	13
	2.3.4.1 Theory - The Requirement	13
	2.3.4.2 Theory - The Alias Filter	13
	2.3.4.3 Circuit Description	14
	2.3.4.4 The Result	14
	2.4 RETURN SIGNAL ANALYZER	15
	2.4.1 Overall	15

TABLE OF CONTENTS (CONT.)

<u>SECTION</u>		<u>PAGE</u>
3	RESONANCE COMPENSATION	17
	3.1 RESONANCE - THE PROBLEM	17
	3.2 RESONANCE COMPENSATION - THE CONCEPT	17
	3.3 EXPERIMENTAL RESULTS	18
	3.4 MECHANIZATION	18
	3.5 OTHER CONSIDERATIONS	20
4	PROGRAMMABLE CONTROLLER	21
	4.1 BLOCK DIAGRAM	21
	4.2 DETAILED CIRCUIT DESCRIPTION	22
	4.3 OVERALL	22
5	FEEDFORWARD CIRCUIT	23
	5.1 THEORY OF APPLICATION	23
	5.2 THEORY OF DESIGN	23
	5.3 CIRCUIT DESIGN	24
	5.4 PLOTS OF THE FREQUENCY RESPONSE vs F1, F2 and INSERTION FACTOR SETTINGS	25
	5.5 SUMMARY	26
6	INTEGRAL COMPENSATION	27
	6.1 THEORY OF INTEGRAL COMPENSATION	27
	6.2 CIRCUIT DESIGN	27
	6.3 APPLICATION EXAMPLE	28
7	ON-LINE DIGITAL DATA TAKING	30
	7.1 THE CONCEPT OF ON-LINE DIGITAL DATA TAKING	30
	7.2 THE POTENTIAL APPLICATIONS OF DIGITAL DATA TAKING	30
	7.3 THE CONCEPT OF DELAY EQUIVALENCE	31

TABLE OF CONTENTS (CONT.)

<u>SECTION</u>		<u>PAGE</u>
8	COMPUTERS AND INTERFACES	33
	8.1 COMPUTER SELECTION	33
	8.2 COMPUTER INTERFACE	34
	8.2.1 The General Setup	34
	8.2.2 Interface for the Corona PC Computer	34
	8.3 THE PC JR INTERFACE BOARD	35
9	COMPUTER PROGRAMS	37
	9.1 GENERAL	37
	9.2 THE FREQUENCY RESPONSE ANALYZER PROGRAM - 'FRA'	37
	9.3 THE AUTOMATIC OPTIMIZATION PROGRAM - Mp	38
	9.4 CONTROLLER ADJUSTMENT - 'RCO'	38
10	THE 'FRA' PROGRAM - FREQUENCY RESPONSE ANALYZER	40
	10.1 GENERAL	40
	10.2 TEST SIGNAL SETUP	40
	10.2.1 Program start	40
	10.2.2 Test Signal Frequency	41
	10.2.3 Test Signal Amplitude	41
	10.2.4 Test Signal DC Offset	41
	10.3 SETUP OF RETURN SIGNAL AMPLIFIERS - SENSITIVITY AND DC REJECT	42
	10.3.1 Channel Sensitivity	42
	10.3.2 DC Reject in Both Channels	43
	10.4 NUMBER OF CYCLES FOR INTEGRATION	43
	10.5 REVIEW OF SETTINGS - LIST	44

TABLE OF CONTENTS (CONT.)

<u>SECTION</u>	<u>PAGE</u>
10.6 TEST MODES	44
10.6.1 Single Point - 'Krun'	44
10.6.2 Continuous	46
10.6.3 Test '1 thru 99 Hz'	46
10.7 RECORDING ON DISC	49
11 THE 'Mp' PROGRAM - AUTOMATIC COMPUTER SOLUTION OF THE OPTIMUM CONTROL SYSTEM PARAMETER ADJUSTMENTS	50
11.1 GENERAL	50
11.2 PROGRAM STARTUP	50
11.3 ADJUSTMENT OF THE RESONANCE COMPENSATION	51
11.4 CHANGE RESET	52
11.5 THE 'name.dat' FILE - SOURCE AND MODIFICATION	54
11.6 INTEGRAL COMPENSATION	55
11.7 PLOTTING THE RESULTS	56
12 THE 'RCO' PROGRAM - COMPUTER SETUP OF THE CONTROLLER AND THE RESONANCE COMPENSATION FOR THREE CHANNELS	57
12.1 GENERAL	57
12.2 PROGRAM STARTUP	57
12.3 THE MENU	58
12.4 TURNING RESET ON OR OFF	59
12.5 CHANGING THE PROPORTIONAL BAND (PB)	59
12.6 CHANGING THE RESET (RPM)	60
12.7 CHANGING THE RESONANCE COMPENSATION	60
12.8 DISPLAY OF PRESENT SETTINGS	60
12.9 EXIT - 'E'	61

TABLE OF CONTENTS (CONCLUDED)

<u>SECTION</u>		<u>PAGE</u>
13	'Dig-Dat' PROGRAM - DIGITAL DATA TAKING USING THE FREQUENCY RESPONSE EQUIPMENTS	62
	13.1 THE MENU	62
	13.2 SAMPLES PER SECOND	62
	13.3 ALIAS FILTER SETUP	63
	13.4 # OF POINTS SETUP	63
	13.5 LIST OF THE SETTINGS	64
	13.6 CHANNEL SENSITIVITY AND DC REJECT	64
	13.7 RECORDING THE DATA ON DISC	65
	13.8 TAKING DATA	65
	13.9 DATA ANALYSIS	66
14	CONCLUSIONS AND RECOMMENDATIONS	70
	14.1 CONCLUSIONS	70
	14.2 RECOMMENDATIONS FOR FURTHER WORK	71

LIST OF ILLUSTRATIONS

<u>FIGURE</u>		<u>PAGE</u>
1-1	Adaptive Controller 'Variables	73
2-1	Frequency Response Analyzer	74
2-2	Test Signal Generator - Block Diagram	75
2-3	Test Signal Generator - Part '1'	76
2-4	Test Signal Generator - Part '2'	77
2-5	Test Signal Generator Front Panel	78
2-6	Input Amplifier - Block Diagram	79
2-7	Input Amplifier - Alias Filter - 1	80
2-8	Alias Filter - Block Diagram	81
2-9	Alias Filter - Input Amplifier - 2	82
2-10	Two Channel Return Signal Analyzer	83
3-1	Channel #6 - Closed Loop	84
3-2	Channel #6 - Open Loop	85
3-3	Channel #6 - Closed Loop	86
3-4	Channel #6 - Closed Loop	87
3-5	Resonance Compensate	88
3-6	Resonance Compensation Front Panel	89
4-1	Programmable Controller Board - Block Diagram	90
4-2	Controller Front Panel	91
4-3	Programmable Controller Board	92
5-1	Feedforward	93
5-2	Feedforward	94
5-3	Front Panel Feedforward Network	95
5-4	Feedforward	96
5-5	Feedforward	97
5-6	Feedforward	98

LIST OF ILLUSTRATIONS

<u>FIGURE</u>		<u>PAGE</u>
5-7	Feedforward	99
5-8	Feedforward	100
5-9	Feedforward	101
5-10	Feedforward	102
6-1	Integral Compensation Compared to Reset	103
6-2	Integral Compensation	104
6-3	Open Loop Frequency Response	105
6-4	Open Loop Frequency Response of Fig. 6-3 on Nichols Plot	106
6-5	One Adjustment of Loop Gain	107
6-6	Fuel Tank Control	108
6-7	Nyquist Plot of Fuel Tank Control	109
7-1	Digital Data	110
7-2	Delay Equivalence	111
8-1	Computer to Mother Board	112
8-2	PC JR Interface	113
9-1	Computer Programs	114
10-1	FRA Set up	115
11-1	Adjustment of Loop Gain - Ch # 1	116
11-2	Adjustment of Loop Gain & Resonance Compensation Ch# 1	117
11-3	Type 3 - Change Reset from 60 to 600 rpm	118
11-4	Reset Changed to 20 rpm Integral Compensation Added	119
11-5	Nichols Chart	120
11-6	Simplified Nichols Chart	121
11-7	Nyquist Plot of 21 FIGURE 11-4	122
12-1	'SETUP.DAT" file for use by 'RCO'	123
12-2	'RCO' - Computer Program of Control Parameters	124

1. INTRODUCTION

1.1- General

It has been recognized that the controllers used to close a load feedback system loop around the electrohydraulic actuators which are used in fatigue and other structural testing were limited in their ability to give the desired control system accuracy and speed of response. It has been the purpose of this contract to significantly improve upon the capabilities of the controller and to show how frequency response methods may be employed in its optimum dynamic setting. This includes the extensive application of computers to automating the frequency response testing and the automatic set-up of the controller functions. We achieved our goals and found the way to a more advanced controller design which in turn would permit the structures testing to be done with greater dynamic accuracy and with higher input speeds. This in turn will permit the tests to be accomplished in much shorter time periods and to have the results be more repeatable.

A companion report has been prepared which describes and presents the software that was written as a part of this contract.

The work done under this contract combined the theoretical with the testing of the results at each stage on facilities at the Structures Test Branch. Thus, the final results are proven, practical, and immediately applicable to the work going on in the laboratory.

The hardware built as a part of this contract permits running a three channel system complete with all of the innovations of the contract. At each stage of the work, flexibility was encouraged to discard the less promising items and substitute items we found we needed as a result of the combined theoretical and practical engineering work.

1.2- The Controller

Figure 1-1A is a block diagram of the present controller as used in the Structures Test Laboratory. The operator can set gain (PB), and reset (RPM). These are the only parameters available to him to achieve the desired level of performance.

Figure 1-1B is a block diagram of the controller as envisaged by the proposal. In addition to the gain and reset functions, it also includes resonance compensation, filter and feedforward networks with all of them under computer control for setup purposes. Later in the contract, we needed to substitute integral compensation for the filter.

Each of the new networks were to accomplish the following:

The resonance compensation greatly attenuates the effect of hydraulic and mechanical resonances upon the closed-loop system permitting much higher gain settings without high frequency oscillation occurring.

The filter was to attenuate line frequency noise.

The feedforward network improves the overall dynamic response and matches the dynamic response of several systems to each other.

The integral compensation greatly improves the loop gain and flattens the frequency response in systems where high spring load constants have greatly reduced the open loop integration.

Each of these networks has two adjustments which, if manually handled, place an intolerable burden upon the operator. Thus, the use of the computer to assist in controller adjustment.

All of the networks may be used together, or any not needed for a given application can be turned off (a gain of 1.0 at all frequencies).

The added compensation circuits use the existing portions of the present controller that are adequate. This includes the load cell excitation and amplification, the servoamplifier, the power supply, as well as the front panel functions, set points, etc. All of the original error determining circuits are also used.

1.3- Frequency Response Measurement

A complete set of equipments were developed to facilitate the rapid, accurate, and meaningful measurement of frequency response. This includes output/input vs frequency and output/error (closed-loop and open-loop) measurements of amplitude ratio and phase shift despite large noise and distortion components.

The frequency response equipment, which is peripheral to and in addition to the main control loop, includes a test signal generator, two channels of input amplification and alias filtering, two channels of read-hold and analog to digital 12-bit conversions timed to occur in synchronism with the test signal. The computer sets up the test conditions of test signal frequency, amplitude, and offset. Then upon command, it takes the two input channels of controller data and uses the data to optimize each controller channel's gain setting, and then to compute (by Fourier Analysis methods) the fundamental of each controller channel's response in amplitude and phase. It completes the computation by taking a ratio of the responses of each input channel to give the amplitude ratio in db and the phase shift in degrees.

The software is such as to permit taking many test points in automatic succession and recording the results on the disc for later use in system optimization.

The frequency response equipment operates from 0.01 hz thru 100 hz, which is the range of interest in this laboratory. The test signal may be set as high as 10 volts peak and as low as 10 mv. peak. The dc offset may be set from ± 10.0 volts to 10 mv with 12-bit resolution, and with a resolution of better than 1/1000 of value in the setting of frequency.

The overall accuracy is well within $\pm 0.25^\circ$ in phase shift and ± 0.2 db in amplitude ratio.

The alias filters are automatically set by the computer to take into account the operating frequency. They provide a minimum of 60 db rejection of the lowest aliasing component.

This equipment and its associated hardware forms an excellent method for rapidly and effectively obtaining accurate and complete frequency response information for later study. It minimizes the expensive test time and conducts the test at low amplitudes where it will not adversely effect the specimen.

1.4- Digital Data Taking

Late in the program we recognized that the frequency response measuring equipments also had a continuous data taking capability that might be helpful in the on-line evaluation of the system response.

An effort was made to develop software for this purpose without requiring any modification to the hardware. Only a limited amount of work was done on this application. We found it to be a very promising capability. While the frequency response equipments are in extended use before the system operates, that is in the setup and adjustment phase, it has no application to the operating mode.

The digital data taking capability puts these equipments to work during the operating mode with the following potential uses:

- 1) To monitor the output and error waveforms and present them on the monitor.

- 2) To check error levels to see if the system should be readjusted and or the program slowed or speeded up.

- 3) To provide the operator with a fast look at any one or more portions of the system as suits the needs of that test.

It should be stressed that this data-taking capability run by the computer could include documentation at regular intervals of the systems performance. Thus, it has an overall supervisory capability when fully developed.

All of the aliasing rejection capabilities of the frequency response analyzer are included with this system. The operator has a great choice between very frequent looks at each parameter (up to 30,000 points per second) to very slow data taking (at 3 points per second).

1.5- Overall Report Organization

The report is organized as follows:

Section 2 is a complete description of the frequency response measuring equipments.

Section 3 is a presentation of the resonance compensation circuits with before and after test data from experiments at the laboratory.

Section 4 is a description of the feedforward circuit and its application and operation.

Section 5 is a description of the programmable controller with reset and gain set by the computer or manually.

Section 6 is a presentation of the integral compensation with an example of an application in a test setup in the laboratory.

Section 7 discusses the data-taking capabilities of the frequency response test equipments for real-time evaluation of system performance.

Section 8 presents the computer hardware and computer interfaces that were used with the equipments above.

Where applicable, each of the above sections includes the theory of the circuit design and the theory of its effect upon the control system performance. Then the circuit is described in detail as well as its implementation, followed by an actual application to a test setup in the laboratory under realistic test conditions.

Section 9 presents an overview of the programs that were written for this job. It shows what each of the programs does and how they relate to each other and to the hardware.

Section 10 is a detailed discussion of the operation of the 'FRA' program which operates the frequency response measuring equipments.

Section 11 is a detailed presentation of the 'Mp' program which uses the test data from the frequency response tests and assists the operator in finding the optimum adjustment of the resonance compen-

sation , the reset, the gain, and the integral compensation.

Section 12 is a discussion of the use of the 'RCO' program to make the adjustments from the computer of the controller settings of gain and reset and the resonance compensation settings of frequency and damping ratio.

Section 13 is a presentation of the operation of the program 'Dig-Dat' which runs the frequency response equipments in the on-line taking of data during operation of the system. This permits on-line evaluation of system performance without injecting a test signal.

Section 14 presents the conclusions reached by the work done under this contract and it includes recommendations concerning where this work logically leads.

2. Frequency Response Measurement

2.1- Basics

Frequency response methods are the most complete and the most satisfactory to apply to closed loop systems such as those used in the Structures Test Laboratory. The open-loop and closed-loop frequency response data quickly shows where a system's performance is inadequate and greatly assists in adding such circuit elements as permit the performance to be brought into line with that desired.

The closed-loop frequency response shows by its bandwidth what frequency components it can follow from the programmed input, and by its flatness how well it will reproduce the input within its frequency limitations.

The open-loop frequency response shows how much loop gain is present at the lower frequencies, and thus how well the system will hold the desired loading, and it reveals where compensation must be added to improve bandwidth, prevent high frequency instability, and add low frequency loop gain.

All of the frequency response theory is based upon isolating the fundamental of the test and response signals and comparing them in amplitude and phase. To this end, Fourier Analysis is employed as the most effective means of rapidly separating signal from signal plus noise.

The frequency response measuring equipment is made up of a test signal generator, two channels of signal amplification, DC rejection, and alias filtering; and two channels of data taking. This is shown in figure 2-1 in block diagram form. These four blocks working with the computer form the entire frequency response measuring system.

2.2- The Test Signal Generator

2.2.1- Frequency and Waveshape

Figure 2-2 is a block diagram of the frequency and waveshape determining portion of the test signal generator. Figure 2-3 is the detailed schematic diagram of this portion. The item numbers such as '3' cross reference on the two diagrams.

Operation starts with the computer commanding a 12-bit input to '1', the digital to analog converter. It uses two input gates to strobe in the upper eight bits and then the lower four bits along with all 12 bits being entered into the output register at one time. A DC output at -10 volts full scale is formed which is directly proportional to the digital input. The D/A converter '1' is used in its upper 50% for maximum accuracy.

The output of '1' is the input to the DC to frequency converter '2'. It has a full scale (corresponding to -10.0 volts) input of 2.0 Mhz. The frequency responds linearly to the input voltage being 1.0 Mhz at -5.0 volts input.

A binary chain of counters is set to count down by the correct factor to give the desired output frequency. The computer does this automatically from the frequency command.

A second set of binary counters are driven by the above frequency input. Their outputs form the address command to the EPROM '5'. The EPROM has been programmed so that its primary address output are bits 1 thru 8 of a nine-bit command to the output digital to analog converter '6'. The high-order bit is provided by the final stage of counting down and corresponds to the sign bit of the twos compliment coding of the D/A converter '6'.

The sinewave is made up of 512 points per cycle which is the same nine bits as the amplitude determining input. This results in much less than 0.5% total harmonic distortion on the sinewave output.

Some of the subtle details can be seen from the schematic diagram of figure 2-3, as follows:

- 1) The binary counter chain is always set by the computer to permit the DC/frequency converter '2' to operate in the top half of the full scale range. This gives accuracy and stability to the output frequency.

2) The use of one-shot '3-7A' gives a very precise timing to the transition from one point to the next on the sinewave.

3) The output from the EPROM is latched into the D/A converter '6' just prior to the counters moving to the next count. This in turn gives the EPROM the maximum time to settle at the new address input before its output is read into the D/A converter. (The EPROM is the slowest link in the loop.) In other words, the data is loaded into the D/A at the leading edge of the pulse '3-7A' and the count occurs in response to the falling edge of the pulse from '3-7A'.

4) A second one-shot '3-7B' is triggered every eighth count to generate 64 commands per cycle of the test signal to convert the input data. This is used as the timing for the return signal analyzer.

5) The EPROM is 16K in size. The sinewave only uses 4K. In another 4K of EPROM, a triangle waveshape is coded. Operation can be commanded here by the computer using the latch '3-1'. Similarly another portion is set with all zeroes so that the computer can command zero output. Additional waveshapes could be made available if they have symmetry about the halfway point (go thru zero at the midpoint).

2.2.2- Output Amplitude and DC Offset

Figure 2-4 is the schematic diagram of the equipment necessary to attenuate the output and add a DC offset in response to computer commands. Twelve bit multiplying DACS (digital to analog converters) are used for this purpose.

The test signal as generated above is the reference input to the MDAC '8'. The output is that portion of the 10.0 volt peak signal as commanded by the 12-bit input to '8'.

The MDACS are two stage devices. They first receive and hold the upper 8 bits of the command. Then they receive the lower 4 bits plus a command to transfer all 12 bits to the output register. Thus the new command level appears all at once and there is no transient in the response.

A precision +10.0 volt reference is the input to '11' where it is inverted and becomes the input to the MDAC '9' and through a 10K resistor to '10'. The scaling is such that with the MDAC at half scale, the DC equivalent input to '10' is zero and there is zero output DC. Scaling the MDAC up and down from the midpoint gives ± 10.0 volt output DC offset capability with 12-bit resolution. Amplifier '10' also sums in the sinewave output of '8'. Thus the final output is a sinewave (or triangle) at the commanded frequency, with the desired attenuation to the commanded amplitude and with a DC offset as commanded thru '9'.

The computer now has the ability to establish a suitable test signal for almost any condition that can be envisaged in the structures test laboratory.

Programming efforts have enhanced this capability by permitting the test signal amplitude to be changed in small steps. This eliminates the case where the sudden application of a large signal amplitude might cause serious upset to the system. Other programs are possible to move the test signal gradually or rapidly from one test condition to the next. The hardware does not significantly limit this approach.

2.2.3- Mechanical

The entire test signal generator was built on one board and assembled with a front panel as shown in figure 2-5. The front panel has test banana jacks for the test signal and for the original full scale test signal. This permits observation of the full scale signal with no output to the item under test, or the use of the fixed output as a reference on such devices as oscilloscopes, counters, etc.

2.3- Input Amplifier and Alias Filter (two channels)

2.3.1- General

Figure 2-6 is the block diagram of the input amplifier less the alias filter. Figure 2-7 is the detailed schematic of the input amplifier less the alias filter.

Figure 2-8 is the block diagram of the alias filter. Figure 2-9 is the detailed schematic of the alias filter.

Note that all of the features of the input amplifier and alias filter are under computer control. This includes the frequency setting of the alias filter, the gain of the input amplifier, and the DC reject of the input amplifier.

2.3.2- Input Amplifier - Gain Setting

The return signal is connected to the \pm inputs of an instrumentation amplifier with a gain of 1.0 volts/volt. This provides very high input impedance, and high common mode rejection of noise, etc. In addition it provides a third input point to perform the DC reject function.

Gain is set by the combination of the fixed gain instrumentation amplifiers '4' and '7' of 10.0 volts per volt and 100.0 volts per volt respectively giving a maximum overall gain of 1,000.0 volts/volt. This in turn provides all of the sensitivity needed by this application. Note that the gain follows the DC reject action and the alias filter so that it only has to amplify the signal and the noise at frequencies below where the alias filter is effective. This often permits much more gain to be used than the nature of the total return signal would permit.

Gain is controlled by the multiplying digital to analog converters (MDAC) '2' and '5'. The computer adjusts their attenuation in steps of times one-half, to give the desired overall gain. By using two of them in series, the MDAC's are operating at the high end of their settings with consequent improvement in accuracy. When they are both set at 1/32 the overall gain is 1 volt per volt. When one is set at 1/16 and the other at 1/32 the overall gain is x2 volts per volt, etc. until when they are both set at unity gain, the overall gain is 1000 volts per volt.

Note that the computer sets the gain in a programmed automatic gain control program. The operator may also select the gain that operation should begin at. Similarly with the DC offset. It is adjusted by the computer as necessary but may be set by the operator as part of the startup procedure.

The output of the input amplifier becomes the input to the return signal analyzer portion of the frequency response analyzer.

2.3.3- Input amplifier - DC Reject Circuit

Many of the operations in the Structures Test Laboratory involve testing at a significant offset from zero load. If for example the test is at -4.0 volts and the test signal is only 50 mv., there would be input amplifier saturation from the DC level long before the test signal was brought up to a reasonable level for analysis. In addition there are test conditions where the DC level may alter a bit during the test. It was decided therefore to make the DC reject action automatic and put it under computer control for all but the initial setting, if the operator so desires.

To increase the resolution of the DC reject, both a +10-volt and a -10-volt reference is available. The computer selects which one is connected as the reference to the MDAC '9' using the programmable switch (with latch) '11'. The actual level of the DC reject voltage is established by the 12-bit command to the MDAC using two commands for the high 8 bits and the low 4 bits with the latter including a shift from the input registers to the output register. Note that the point where the DC reject signal is summed into the amplifier '1' is a gain of +1 volt per volt point.

Normally a change in the DC reject level is made by the computer at the end of a run when the DC level of the return signal is also evaluated and a decision is made as to whether and by how much to change the DC reject setting to reduce the net DC level at the output of the input amplifier. This sequence occurs with every measurement.

2.3.4- Alias Filter

2.3.4.1- Theory - The Requirement

Digital data taking - or sampling - always causes a reading of frequencies at the input which are at the sampling frequency or at multiples of the sampling frequency to be folded back to DC plus the difference of the noise frequency from the sampling frequency or multiple of the sampling frequency. This is known as an aliasing error. For example if the frequency response analyzer were sampling at 1,000 samples per second (corresponding to a test frequency of 15.625 hz and 64 points per cycle), then a noise term at 1015.625 hz would emerge from the sampling as another component of the 15.625 hz return signal. For the precise use of the frequency response analyzer, this is an intolerable situation that can only be corrected by the insertion of an aliasing filter.

2.3.4.2- Theory - The Alias Filter

The test signal is generated with 512 points per cycle. The command to take data is generated every eighth point, or 64 times per cycle of the test frequency. Thus the sampling rate is 64 times the test frequency. No matter to what value the test frequency is set, the sampling rate remains tied to it. Thus the alias filter must also be tied to the test frequency.

The alias filter is a low pass second order filter which has its break frequency set at twice the test frequency. Means are used (as described below) to keep the alias filter break frequency and thus its phase and amplitude response to the test frequency return signals constant.

The output/input of the alias filter is as given below in equation 2-1.

$$\text{Output/Input} = \frac{1}{1 + j \frac{f}{f_t} + (j \frac{f}{2f_t})^2} \quad 2-1$$

where f_t = test frequency
 f = frequency

2.3.4.3- Circuit Description

Reference is made to figure 2-8 for the block diagram and to figure 2-9 for the circuit diagram of the alias filter. Common parts have the same number in the two diagrams.

The frequency range of operation is selected by the RC combination of amplifiers '22A' and '23A' which are always set to matching values. A programmable latching switch as commanded by the computer '22' and '24' set the input resistor from R1 R2 R3 and the feedback condenser as C1 or C1 & C2 in parallel. The lowest frequency range corresponds to 1.0 meg and 1.0 microfarad.

Within each frequency range, the actual frequency is set by the multiplying digital to analog converters (MDACS) '21' and '23'. These are set by the computer using a 12-bit command to correspond to the fraction of full scale of the frequency range of operation. For example, a test frequency of 8.0 hz would correspond to a setting of 0.80 on these MDACS.

In this way, the alias filter is kept set to the same relative position (twice) with respect to the test frequency regardless of the operating frequency and without operator intervention. It is handled automatically by the computer as a part of its frequency setup procedure.

2.3.4.4- The Result

The alias filter is at $1/32$ of the test frequency. Since it is a quadratic filter, it attenuates signal components at the test frequency of $(32)^2$ or by over 1000/1. This should take care of almost any aliasing noise term that might otherwise have ruined the results. Note that it completely eliminates still higher harmonic terms.

In addition this attenuation of all high frequency noise greatly improves the operation of the frequency response analyzer when there is high frequency noise present. The gain of the input amplifier can be increased because it will not saturate from the high frequency noise terms.

2.4- Return Signal Analyzer

2.4.1- Overall

The return signal analyzer performs the following functions:

- 1) It employs a read/hold circuit to capture the input signal amplitude at exactly the time commanded by the test signal generator.

- 2) It employs a high speed (10 microsecond) digital to analog converter which generates a 12-bit conversion of its analog input.

- 3) It has latches which hold the output of the analog to digital converter and sequence the 12 bits to the computer upon command (the computer takes only 8 bits of data at a time).

- 4) There are two identical channels of the above, which operate in synchronism to simultaneously handle two channels of input signal from channel 1 and channel 2 of the frequency response analyzer.

2.4.2- Circuit Details

Figure 2-10 shows the detailed schematic of the two channel return signal analyzer. When channel 1 is discussed the equivalent part in channel 2 will be in parentheses.

The 'take data' pulse from the test signal generator causes the flip-flop '33B' to clear which in turn puts the track-hold circuit '1' ('21') into 'HOLD'.

The end of the take data pulse also causes the start of the analog to digital conversion process in '2' ('22').

The end of the conversion is signaled by the EOC pin 20 of '2' ('22') and the last one completed causes the flip-flop '33B' to return to its original state. The track-hold circuit is returned to track. At the same time, the EOC signal from the A/D also causes the registers '3' & '4' ('23' & '24') to load the 12-bit outputs into their outputs. The input conversion system is now ready for the next point.

The computer is signalled that the conversion is completed by the output of flip-flop '33A' which was also clocked by the EOC signal. Its output is on the high-order bit of the return bus 'B'. The computer monitors this bit and when it goes plus, it takes the data from the four latches '3', '4', '23', and '24', as follows:

1) The computer sets the lowest two bits of bus 'C' to 00 . This causes the decoder '32' to make pin '4' low (decoding a zero) which in turn turns on the output of register '3'.

2) The computer reads in the 'B' bus.

3) The computer then outputs 01 to the C Bus. The decoder '32' causes pin 5 to go low (decodes a 1) and pin 4 returns to its high state. The output of latch '4' is now active on the bus. The computer reads it in.

4) The computer repeats the procedure for the reading in of the output of '23' and '24' in turn with bus 'C' set at 10 and then 11 to be decoded in turn as 2 and 3. The computer then has the complete results of the last point in its memory for later processing and it returns to checking the high order bit of bus 'B' so as to know when the next measurement is completed.

Note the following:

1) When the second point is read, the data flip-flop '33A' is cleared so the high-order bit goes to zero. This also permits the computer to check that the sequence is correct.

2) Bit 6 (the second highest bit) is used to give the computer information as to whether the cycle is in its first half or second half (0°, or 180°). This permits the computer to establish the correct phase of the signals with respect to the test signal in its data reduction procedure.

3) The 12-bits output of each converter is transmitted as two 6-bit portions as each register is read by the computer.

The entire procedure is automatic and occurs without the operator being involved. The computer establishes how many points to take for each run (minimum of 64 with multiples for integrating over more than one cycle of the test frequency). The track-hold and conversion equipments continue to operate even though the computer is not reading the data.

3.- Resonance Compensation

3.1- Resonance - The Problem

The combined effect of the nature of the structural impedance being driven by the electro-hydraulic actuators, and the dynamic characteristics of the hydraulic cylinder often cause resonance at high frequencies (as much as 100 hz) that have very low damping. We will show that these resonances dominate the situation when the operator tries to raise the gain in the closed loop loading system. If the operator tries to make a reasonable adjustment, the loop goes into oscillation at the resonant frequency. The operator is forced to accept a very low loop gain to prevent this oscillation from occurring under all of the operating conditions. This in turn reduces the closed loop response, and forces the program to be run at slow speed. In addition, the response may still be very noisy and the results will not be highly reproducible.

To some extent the problem can be reduced by such strategies as eliminating hoses from the servo-valve to the actuator (hard pipe the servo-valve on the actuator) but even then there are loading situations that are kept from satisfactory operation by the characteristics of the load. These cannot be altered

3.2- Resonance Compensation - The Concept

We determined that the problem could be corrected by adding a second-order low-pass filter with adjustable resonant frequency and damping ratio to the controller, as a part of the open-loop system. The filter, referred to as the resonance compensation circuit, is set high enough in frequency so that it permits the closed-loop control system to have high dynamic performance and yet low enough so that by the structural resonances there would be a great deal of attenuation in the open-loop frequency response. The structural resonances would be sufficiently attenuated so that even with large variations in the damping ratio and the resonant frequency, they would have little or no effect upon the closed-loop system's response. This would give a clean and accurate response in the system to the program and the programming speed could be increased.

3.3- Experimental Results

Figure 3-1 is the open-loop frequency response taken on the wing test structure at position 6. There is a response everywhere above 10 hz that is high and in the region above 80 hz the output/input exceeds unity by a great deal. Further it was not possible to set the loop gain high enough to make the low frequency closed-loop response equal to unity. This was a very unsatisfactory result.

Figure 3-2 shows the open-loop frequency response for this system. It is clear that an equivalent integration occurs to 10 hz but beyond that point the structural and hydraulic resonances take over and the gain stays high with an increase out near 100 hz. This causes the effects of fig. 3-1.

With resonance compensation added to the controller, and with the frequency set at 50 hz, and the damping ratio at 1.5, the closed-loop frequency response of figure 3-3 results. This shows a marked improvement above 30 hz with a very rapid falloff in the amplitude ratio. There is greater flatness in the low frequency region. All of this would give a much smoother and more accurate dynamic response. It also gives much less interaction of the other control loops into this one and vice versa.

Reducing the resonance compensation frequency to 23 hz and using the damping ratio of 1.5 gives the results of figure 3-4. The low frequency closed-loop response is even flatter and the cutoff at the high frequency region starts sooner and is steeper.

Several other cases were tried and where there was a problem with high frequency structural and hydraulic resonances, the resonance compensation was effective in achieving a much more satisfactory adjustment of the control system's dynamic response.

3.4- Mechanization

Figure 3-5 is the circuit diagram of the resonance compensation circuit that is both manually operable from the front panel and computer settable in frequency and damping ratio. Figure 3-6 is the front panel diagram showing the controls and test points.

Note that the circuit for the resonance compensation is in many ways similar to the alias filter as presented in section 2.3.4 except that both the frequency and the damping ratio can be programmed.

The integrators in the loop are amplifiers '16' & '17'. Their input resistor ' R_1 ' and feedback condenser ' C_1 ' are set for a full scale frequency of 50 hz. This frequency is high enough so that it will not prevent the test systems in which it is used to lose performance.

Frequency is set as a fraction of the full scale value by the 12-bit multiplying digital to analog converters (MDACS) '9' and '10'. They are set by the computer in automatic mode and by the counters '1', '2', & '3' in manual mode.

The damping ratio is full scale of 2.0 which was found to be desirable in our experimental program. It is adjusted by the 12-bit MDAC '12' to as low a value as desired. Normally this is not set below 0.5.

In an effort to give the operator a calibrated reading of the setting of the resonance compensation MDAC '11' is provided to give a DC voltage that directly reads in frequency with 5.0 volts = 50 hz; and MDAC '13' gives a direct readout of damping ratio with 2.0 volts corresponding to a damping ratio of 2.0.

To give the unit manual operation an auto-manual switch S13 for frequency and S14 for damping ratio is provided. When in automatic, the computer sets the count into the respective counter chip as an initial condition ('1', '2', '3' for frequency and '5', '6', '7' for damping ratio). When in manual, the switches enter a count into their respective counter in either the 'up count' or 'down count' input so as to move the setting by one count, 16 counts or 256 counts per switch depression. Thus the operator may make fast or slow changes in the settings to see what effect they have on the results (or the operator may use the computer programs to change the settings).

A plus and a minus output was generated so that the network could be put into the loop without changing any other setting.

3.5- Other Considerations

Because of the extensive testing that might be required before a resonance compensation circuit could be properly adjusted, a program was developed to take the experimental data and using the computer to automatically find a desirable adjustment of the frequency and damping of the resonance compensation. This is discussed in section 12.

It must be stressed that in multiple loop-loading situations which is the most common one encountered in the structures laboratory, the benefits of this network multiply in those instances where they are needed. As the response of each of the control loops to high-frequency input is greatly decreased, they introduce less of this type of upset to the other control loops in the overall system and the entire loading system becomes more accurate, more smooth and its dynamic response is improved. Since 60 hz and 120 hz response is greatly attenuated, this also simplifies the normal power line noise problems in setting up the equipments. The entire test setup becomes easier to manage and gives better test results in a shorter period of test time.

4- Programmable Controller

4.1- Block Diagram

Figure 4-1 is the block diagram of the Programmable Controller unit. Figure 4-2 is the front panel showing the controls and check points. Figure 4-3 is the detailed schematic of the Programmable Controller unit.

The Programmable Controller was designed and three were manufactured to permit computer setup of gain (from 100 volts per volt to 0.1 volts per volt) and reset from 6 RPM to 6000 RPM. All of the setup can also be done from the front panel by the operator in manual mode.

As shown on figure 4-1, ICs '6' and '7' perform the gain function. '7' is an instrumentation amplifier set at a gain of 100.0 volts per volt. '6' is a multiplying digital to analog converter (MDAC). By setting the 12 bits any desired attenuation of the input signal can be had from 1.0 (all 12 bits set high) to lower than .001 (third lowest bit set high only). When combined with the fixed gain of 100.0 volts/volt of '7', the net gain applied to the error signal input ranges from 100.0 to less than 0.1 volts per volt with 12-bit resolution. This gives the computer a very precise way to set the loop gain.

ICs '8' and '9' aided by the operational amplifiers of '8A', '11' and '12' provide the programmable reset function that can also be turned off when so desired.

The reset range is determined by the programming of the latched switch '9'. It connects R1, or R2, or R3 as the input resistor to '12A' with a fixed feedback capacitor of 1.0 microfarads. With 1 megaohm input resistor 'R3' connected, the peak RPM is 60. With 100K ohms connected 'R2', the peak RPM is 600 and with 10K ohms connected 'R1', the peak RPM is 6000. If the switch is programmed to connect 'R0' around the condenser, the reset action is turned OFF.

IC '8' controls the fraction of the peak reset value set by the range from the full-scale value down to 0.1 of the value. Using 12-bit setting of the fraction it has great accuracy and resolution.

Note that changes in the reset do not bounce the output.

When the reset is off, the signal path is through the unity gain element '11A' only.

4.2- Detailed Circuit Description

ICs '1', '2', '3', and '4' as shown on figure 4-3 provide the means to set up the controller from the computer or the front panel.

When SW1 is set on automatic, the outputs of the drivers '1' and '3' are made active. This connects the computer bus 'A' and 'C' to the inputs of the MDACs and to the programmable switch. This makes the functions and their values programmable by the normal computer methods.

When SW1 is set on manual, ICs '1' and '3' are put into their standby mode and ICs '2' and '4' are turned on to drive the MDACs and the programmable switch. The desired data is setup on SW3 and the desired function is selected by SW4. Then the enter switch SW2 is depressed and the function is programmed. The procedure is repeated for all five functions when all of the parameters are to be changed.

Test points are provided at the output of the gain setting and at the output of the reset.

4.3- Overall

This circuit was used to replace the controller board in the controller. With it the computer was able to control the gain and the reset. We did not attempt to compare the performance of the two controllers. In theory, the programmable controller has more gain and reset accuracy and resolution than the present board; the reset has more range (both at the high and low ends); and the stability using the instrumentation amplifier '7' as the gain element is much greater with less noise.

5.- Feedforward Circuit

5.1- Theory of Application

The feedforward circuit is added to the control system as shown in figure 5-1. The program is passed through the feedforward circuit and then becomes the input to the control system. Normally the feedforward circuit has a gain of 1.0 at all frequencies.

The control system is setup to come as close to the desired performance as possible within the limitations of the closed loop system. Frequently this closed loop adjustment has some deficiencies.

These might include:

- 1) Having a dip in the output/input vs frequency or a rise in the output/input vs frequency that in turn produces distortions in the response to the programmed input, or limit the speed of the input program.

- 2) Having a significant difference in the frequency response of several of the control systems, so that the overall multi-system response is set by the slowest system.

- 3) Having inadequate bandwidth in the closed loop response.

All of these situations and more can be significantly improved by using the characteristics adjusted into the feedforward network to give a net control system output/programmed input that is desired.

The feedforward network provides the means to precisely adjust out relatively small discrepancies in the closed loop frequency response permitting much improved net response of the system. The goal of accurate reproduction of the input waveform can be achieved in more cases and several control loops can be brought into improved synchronization.

5.2- Theory of Design

As shown in the lower portion of figure 5-1, each feedforward circuit has three controls. These are: the frequency break of the lead term, the frequency breakpoint of the lag term, and the insertion factor.

The lead break frequency ' f_2 ', sets where the lead term ends (in the asymptotic approximation). The lag break frequency ' f_1 ' sets where the lag break frequency starts. The insertion factor ' K_2 ' sets how far the attenuation or amplification will go in the frequency range between f_1 and f_2 as allowed by the separation of the two settings. (Attenuation when $f_1 > f_2$ and amplification when $f_2 > f_1$).

With these three adjustments the operator may set the exact contribution of the feedforward circuit to the frequency response of the control system.

5.3- Circuit Design

Figure 5-2 shows the circuit design of the feedforward unit. Figure 5-3 shows the front panel design of the feedforward unit. This unit was built to operate in manual mode only. The computer cannot set the feedforward settings. The operator must do so.

The direct path from input to output is through U4 with a gain of +1.0 by using the pin 2 input to U4. Anytime that the insertion factor is set at '0', this is the only path that the signal input follows to the output. Because this gain is +1.0 volts per volt, the use of the feedforward unit does not change the system response as long as the insertion factor is set at '0'.

The ICs U1 and U5 form a closed loop that generates the lag term. The ICs U2 and U6 form a closed loop that generates the lead term. U7 corrects the gains so that the feedforward networks always have unity gain at the frequencies below and above the frequency range in which it introduces a change (primarily from $f_1/(1-K_2)$ to $F_2(1-K_2)$) in the frequency response.

R1C1 determines the maximum lag frequency of 5.0 hz. R2C2 sets the maximum lead frequency of 5.0 hz. Setting R_0 down from its full scale setting reduces the lag frequency setting from 5.0 hz linearly to 0.5 hz. There is a calibration on the front panel of the settings. Setting R_3 down from its maximum reduces the lead frequency setting from 5.0 hz down to 0.5 hz. There is a calibration on the front panel of the settings.

R4 sets the insertion factor. The '0' position is shown on the front panel. R4 can be adjusted to an insertion factor of 0.5. This permits a ± 6 -db adjustment in output/input vs frequency (when the lead and lag terms are sufficiently separated). This is presently projected as the maximum correction that should be attempted with the feedforward unit.

R4 is a dual ganged potentiometer to permit the correct gain of 1.0 to be achieved outside of the range of operation of the feedforward unit.

5.4 - Plots of the Frequency Response vs f_1 , f_2 , & Insertion Factor Settings

Figs. 5-4 through 5-10 show various aspects of the effect of parameter adjustments upon the frequency response of the feedforward unit. These should give the operator an insight into what can be accomplished with the feedforward circuit.

Figure 5-4 shows the widest possible adjustment with the lead set at 0.5 and the lag set at 5.0 for several values of insertion factor. All of the previous asymptotic approximations now give way to the actual response of the networks and their interaction. Observe that there is some gain from very low frequency and the gain persists to a high frequency. This is in keeping with the system being corrected. There are no sharp and narrow ranges of need for correction. Rather there is a worst-case area with a slow return to its desired values.

The setting of the insertion factor = 0.5, gives a maximum gain of +5.4 db. Note, however, that with the insertion factor set at 0.1, the maximum gain is only 0.8 db. The operator can readily set below 0.1 (20% of full scale) and so can correct for very small attenuation with this circuit setting capability.

Figure 5-5 shows the effect on the results of the first curves of moving the lead setting to 1.0 hz. for three values of the insertion factor. It is apparent that the range of frequencies (at the low frequency end) over which there is significant gain change has been narrowed and that the maximum gain has been reduced.

Figure 5-6 has the lead term increased further to 2.5 hz for insertion factors of 0.1, 0.3, and 0.5. It is evident that again the gain introduced by the network at the low frequency end has been reduced and the peak gain introduced by the network has been decreased. In other words, the operator may reduce the range of frequencies over which the feedforward network introduces gain change by making the lead and lag terms more nearly equal.

Figure 5-7 shows the effect of having the same ratio of lead to lag settings as in figure 5-6 but with the settings at 0.5 hz for lead and 1.0 hz for lag for the three values of the insertion factor.

It is apparent that the results are the same for the two cases except that it is centered at the lower frequencies as set for figure 5-7 compared to figure 5-6. Thus the operator should note that the ratio of the two settings of lead and lag is critical as to how much effect the insertion factor will have.

Figure 5-8 shows what happens when the lead and the lag settings are equal at 1.0 hz. Because the lead term actually starts its action at its setting ' f_2 ' times $(1-K_2)$ and because the lag term stops its action at ' f_1 ' divided by $(1-K_2)$, equal settings does not produce zero output, but gives the results as shown for different settings of the insertion factor. Note in particular how a small change can be made using this circuit.

Figure 5-9 is another plot of the frequency response of the feedforward network with the lead setting of 1.0 hz and the insertion factor held constant at 0.3 for three values of lag (1.0 hz, 2.0 hz, and 4.0 hz). It is obvious that as the spread between the lead and lag terms increases, the gain curve covers a wider range of frequencies and is higher in value in the midrange between the settings. This matches the need, as in most cases the broader the range of frequencies to be corrected, the larger the correction needed. If not in a particular case, then the insertion factor can be decreased.

Finally, in figure 5-10 an attenuation curve is plotted which shows the resulting frequency response of the feedforward network when the lag term is set to break at a lower frequency than the lead term. These curves are nearly identical with the inverse of the previous sets with the same rules for setting of insertion factor and for the effect of the spread in the lead and lag settings, only now it is the amount of attenuation that is introduced and the frequency range over which it occurs.

5.5 - Summary

The feedforward circuit permits the operator to make small improvements in the control system response to the programmed input without fear that it will seriously overcorrect and with an unusual ability to make small corrections in the frequency range of interest. This is a new and highly useful device in the extension of the dynamic accuracy of the loading systems. It also takes a great deal of pressure off of very difficult closed loop adjustments to achieve the equivalent results.

6.- Integral Compensation

6.1- Theory of Integral Compensation

At the very end of the program, it was found that the Structural Test Laboratory encounters a type of system which has an open loop frequency response that cannot be adequately improved by the use of the controller functions that have been made available thus far. Upon careful study, it was found that this type of loading situation needed what is called integral compensation.

Figure 6-1 is a plot of the amplitude ratio and phase of reset and of integral compensation. Reset is seen to be a special case of integral compensation.

Consider the reset curve first. At low frequency, the reset introduces 90° of phase lag and attenuates at 6 db for each doubling of frequency. Then at the higher frequencies (from 0.1 and higher) the phase lag diminishes toward zero, and the rate of attenuation also decreases to zero.

The integral compensation has a second adjustment. The operator selects the frequency at which it starts as well as the frequency at which it stops. In so selecting, the operator also limits the maximum phase shifts and the range of frequencies over which it has an effect. Thus it can be inserted to compensate for a deficiency in a portion of the system open-loop response and shape it as desired. This technique is widely used in instrument servomechanisms and high performance electro-hydraulic control systems. It is not used in industrial controls.

6.2- Circuit Design

Figure 6-2 is the circuit diagram of the integral compensation. The circuit was made by modifying the feedforward unit. The circuit operates as follows:

'U1', 'U5', and the associated components form the lag term which breaks at ' f_1 '. The maximum value of ' f_1 ' is set by R1C1 at 0.16 hz. Adjusting K1, the front panel adjustment of lag permits ' f_1 ' to be decreased to as low as 0.016 hz.

'U4' and K2 set the separation of the lead term from the lag term. It can be set from '0' at which point the integral compensation has unity response at all frequencies, to 20 where the response follows that for $\omega = 20$ of figure 6-1.

The circuit is derived from the feedforward circuit. A switch is provided at 'U4' which permits the gain to be increased by 10 times. This adjusts for the effect of the integral compensation on the need for loop gain.

The circuit was built on the feedforward board and is manually adjustable.

Note the extreme simplicity of the circuit as it finally developed.

6.3- Application Example

Measurements were made on the open-loop frequency response of the wing fuel tank setup at the laboratory. This loop had been particularly troublesome in obtaining a satisfactory adjustment with the standard control equipments and capabilities.

Figure 6-3 shows the amplitude ratio and phase shift vs frequency and in figure 6-4 the same data is shown plotted on Nichols graph paper with each point being the amplitude and phase at a given test frequency. Finally, figure 6-5 shows the Nichols chart superimposed on the plot to show the closed-loop response from the open-loop data for one loop gain setting.

Figure 6-5 clearly shows the problems in adjusting this control system. The low frequencies (0.1 hz) have very low loop gain. They also have an output/input that is greater than unity and will increase if the loop gain decreases. There is a broad range of frequencies (0.2 to 0.4) with very low loop gain. This in turn means very poor following of the input command. Finally, the system is sensitive to an increase in loop gain which will rapidly give large values of the peak output/input. In short, at best this system will not perform well, and if not adjusted exactly, it will perform very badly.

Changing the reset to 600 RPM, gives the results shown in figure 6-6. There has been some improvement in the loop gain at low frequency, but the overall bandwidth is low (1.6 hz) and the adjustment is still too critical and the low frequency gain is still unsatisfactory.

Adding integral compensation with break frequencies at 0.1 and 1.0 hz and using reset of 20 RPM gives the response shown in figure 6-7. The bandwidth has been increased to 2.8 hz. The low frequency loop gain has been substantially increased. The loop gain setting is much less critical. This system will perform the following of the program in a much more satisfactory manner than the others. Thus, integral compensation is a valuable tool in adjusting some of the control systems in the laboratory to meet their requirements for high speed, high accuracy following of the programmed input.

The predictions of this section were borne out in practice and the first designs of the integral compensation units are in use in the laboratory.

7. On-Line Digital Data Taking

7.1- The Concept of On-Line Digital Data Taking

Late in this program, we realized that the same equipment that was developed for frequency response measurement could also be used to monitor the on-line behavior of the signals within the control systems such as load vs. time, error vs. time, etc.

Figure 7-1 shows the basic concepts. Because there are two channels of signal amplification, filtering and analog to digital conversion equipment in the equipments, two signals can be converted to their digital equivalent at the same time. As shown, there is a programmed input to the loading system and the output from the load cell being digitized at times 1,2,3 etc. The digitized signal is being put into memory and can, at the operator's command, be recorded on disc.

The operator in this type of signal recording must select the number of points per second to be taken, the setting of the alias filter, the scale factor of each channel and the DC offset of each channel.

7.2- The Potential Applications of Digital Data Taking

It was envisaged that digital data taking had several possible applications to the work in the Structures Laboratory.

First, it offered a method of continuously monitoring the signals as an on-line method to insure that operation was within limits in a more sophisticated manner than error and load limits now provide.

Second, it offered the possibility of on-line system adjustment to improve the performance or to change the program speed when dynamic error levels were too high or too low.

Third, it offered the possibility of generating a new error criterion. This involves considering the best match of the delayed response of the system under test to the input which gives an error signal that is more meaningful to the application of fatigue testing and might permit higher programming speeds. This concept is explained in detail in section 7.3

Fourth, it is readily expanded to give a more complete and precise monitoring of the entire fatigue test operation than that provided by the recordings now in use.

7.3- The Concept of Delay Equivalence

Reference is made to figure 7-2 which shows the concept of delay equivalence.

Any system that is reasonably linear, and is operating in a well setup closed loop configuration (almost always achieved with the additional control functions provided as a part of this contract; that is, resonance compensation, integral control and system setup based on careful frequency response measurement and adjustment), has a near linear phase lag vs. frequency in its operating frequency range. The slope of the phase response (phase change/frequency change) is an equivalent time delay expressed in seconds.

As long as the input test signal is limited in its frequency content to this frequency range (and this is the usual operating mode in the laboratory), the output will replicate the input, but with a delay in time as given by the above calculation. Thus, while a significant error level exists within the control loop, a precise comparison of the output, delayed by the computation above of the delay equivalence, with the input would give a much smaller error level. This is the true error between what the load experiences as its load program versus what it is programmed to experience. Of course in multi-loop test setups the individual loops would have to be adjusted with nearly the same equivalent delay for this thinking to be valid. With the assistance of the feedforward network and careful setup this should be readily accomplished.

The digital data can be moved in time by the value of the time between points or any multiple thereof. For example, if the setup is adjusted by the operator to take 1,000 points per second, the data can be moved in 1.0 millisecond increments to see where the best overlap occurs. In fact this method of error generation might be made on-line as well as after each data taking period.

In short, the digital data-taking procedure might allow the most precise matching of response to input on a dynamic basis using a best fit based on inserting a delay equivalence in the data of the output with respect to the input.

If we put this system into operation we might see a significant increase in the allowable speed at which we might run the systems. This would give us an improved picture of the loading the specimen had actually been subjected to.

Section 13 has a description of the program which performs this digital data taking as far as it was developed under this contract.

8.- Computers and Interfaces

8.1- Computer Selection

The original proposal upon which this contract was based, called for the use of a portable computer as the basis for all of the work that was to follow. An extensive effort was made to identify a small portable computer that would be usable for the entire job. We found that the ones available at that time were not satisfactory. The rising tide of the personal computer of the IBM type, or at least compatible with the IBM PC, was visible and clearly showed that the computer we selected should be of that type. This insured that software and add-on hardware would also be available and further insured that repairs and replacement parts would remain in stock and available.

The Corona Model PC21 was purchased along with a keyboard, a monitor, dual double sided double density disc drives, and 512K of memory. The software included MS-DOS, GW Basic (not used) and Multimate (not used). This computer was not portable but had all of the capabilities needed for work at DRF, Inc. and it was to be delivered to the Structures Laboratory later.

For output to the controller parts and to the frequency response analyzer, a Ziatech ZT1488 Multifunction Controller Board was obtained with a ZSBX30 plug-in which provided the necessary parallel input-output lines needed for the job.

At a later date, when it was necessary to bring a computer to the Structures Laboratory at WPAFB, an IBM PC Jr. was acquired along with its monitor, keyboard and dual disc drives. The small size and light weight of this unit made it possible to carry it back and forth on the field trips. The modes of operation were identical, which made it possible to use almost identical software in the two systems.

At no point did the performance of the computers compromise the needs of this application.

8.2- Computer Interface

8.2.1- The General Setup

We decided to base the communication between the computer and the equipments to be developed under this contract upon a parallel bus structure with three 8-bit busses; designated 'A', 'B', and 'C'.

The 8-bit 'A' bus is the data bus. It transfers the desired values of the setup of the components of the control system to each part.

The 8-bit 'B' bus is used exclusively to transmit data back to the computer. This is primarily for the frequency response analyzer when it is taking data.

The 8-bit 'C' bus is used to select which function on which board is to be the recipient of the data from the data bus 'A' and to cause it to be entered there; and to identify which data will be transferred to the computer on the 'B' bus.

8.2.2- Interface for the Corona PC Computer

Figure 8-1 is the schematic diagram of the interface board from the Corona computer to the mother board of the equipment enclosure of the control and frequency response measurement equipments.

The 8 bits from port 'A' are buffered by '1' which then drives all of the inputs requiring the data input.

The return signals for bus 'B' are buffered by '4' to drive the lines to the computer.

The 8 bits of port 'C' are buffered by '2' and then used as follows:

The three lowest bits from pins 18, 16, and 14 of '2' are used on each of the boards for function select. That is, they drive 3-bit to 8-bit decoders to select which one of up to 8 functions on each board will be driven to the value set in the 'A' bus.

The three bits 4, 5, and 6 (pins 9, 7 and 5 of '2') of port 'C' select which board is to receive the data; along with the bit 3 and bit 7, as follows:

The three bits 4, 5, 6 drive the input of two three-to-eight decoders '3' and '5'. The output commanded by these three bits goes low when the respective enable input (pin 4 of '3' or '5') goes low.

IC '3' selects boards numbered 0 through 7. IC '5' selects boards numbered 8 through 15. Normally bits 3 and 7 of port 'C' are kept high. When the board is commanded the respective bit is taken low. This drives one line of the mother board low which is in turn responded to by the board wired to the line. For example, board #4 would respond to the line of $\bar{a}27$ going low.

This permits any board to be plugged in at any location and yet to be commanded by the computer in exactly the same manner. The mother board is a complete parallel connection system to all of the boards.

The programming is arranged so that the operator does have to establish, for the computer, which board is in which system. The position of the board in the assembly does not have to be established. The computer program takes care to manipulate the 'C' port to properly select the board and function which is to receive the data on the 'A' bus and to enter it into the selected register on that board.

This system has all of the flexibility needed by the job.

8.3- The PC Jr Interface Board

The PC Jr did not have a parallel port plug-in unit as required by this application. We therefore decided to attach directly to the connector of the computer and to copy the interface for a set of three parallel ports. This was done with ICs # '1', '2', '3', '4', '6', & '7' of figure 8-2. In brief the functions being performed are as follows:

The comparators '6' and '7' establish the address at which the interface will respond to input and output commands from the computer (port number).

IC '4' is the transceiver which buffers the computer data bus and the data bus to the 8255 ('1').

IC '2' buffers the low two address bits and the IOR and IOW signals as they drive the 8255, and the transceiver '4'.

IC '3' provides the logic that drives the chip select line of the 8255 when the address, etc., is as desired and which buffers the RST line of the 8255.

The 8255 (IC '1') is a complex unit that responds to the inputs and loads internal registers to give the three 8-bit port outputs in response to the computers output and input commands. They correspond exactly to the three ports made available by the Ziatech equipments as described in section 8.2.

ICs '11', '12', '13', & '14' provide the same functions as those of their counterparts on figure 8-1. They buffer port 'A' the data port; buffer port 'B' the input port; and buffer and select port 'C' the function and board select port. Note that only the lower 8 board selects are provided because of the use of this equipment with a limited number of the control units in the Structures Laboratory.

9.- Computer Programs

9.1- General

We decided to make use of multiple programs to accomplish all that was needed in this contract rather than try to put it all in one program. The reasons for this will become clear as the description of each program and its range of application is brought out below.

Figure 9-1 shows the basic interrelationship of the programs.

9.2- The Frequency Response Analyzer Program - 'FRA'

The frequency response analyzer program operates the frequency response measuring equipments as previously described in Sec. 2. The 'FRA' program permits the operator to set all of the test conditions of test signal frequency, test signal amplitude, test signal DC offset. In addition the operator selects the number of cycles over which the signal analysis is to take place, the sensitivity of each of the return signal channels, and the DC reject levels of each of the return signal channels. Finally, the operator makes decisions concerning whether the test is to be run once, or to be a part of a series of test points, or to be repeated until told to stop and the operator decides whether or not to record the results on the disc. Each of the settings except that of test signal amplitude and frequency has a default value that will occur if the operator does not enter values. In making the measurement, the system will automatically adjust the sensitivity of each channel and the DC reject of each channel to insure good results.

Upon command by the operator, the computer starts the frequency response measurement, accumulates the data, and reduces the data to the form of amplitude ratio and phase shift of the two channels with respect to each other.

If disc records are made of the results, two files are formed. One, xxx.gen, gives all of the data as presented on the monitor. The other, xxx.dat, holds the results in a form that is usable by the automatic optimization program, 'Mp', as described in the next section.

The complete 'FRA' program is detailed in Sec. 10.

9.3- The Automatic Optimization Program - 'Mp' -

This program permits the operator to study the data file, xxx.dat, taken by the frequency response analyzer for the following:

The program computes and lists the output/input vs frequency for the open-loop data in the file at each of the test points when the loop is closed with a gain such that the peak value of output/input = 1.0 (0 db). The gain necessary to achieve this result is also given.

The program then permits the operator to add a resonance compensation circuit to the open-loop controller and to adjust it for near optimum results. The operator only has to chose the desired bandwidth. The program tries several settings of the resonant frequency and then the damping ratio until it finds one that gives the desired bandwidth with peak value of output/input of 1.0. The complete open-loop and closed-loop results are listed for the operator to check.

The operator may then try different settings of the reset (rpm) and have the program present him with the effect upon the resulting open-loop and closed-loop results. After changing the reset from that used in the test, the operator may also redo the resonance compensation optimization. In many systems this will suffice to find the desired settings of open-loop gain, reset (rpm), resonance compensation, frequency, and damping ratio. These can then be put into the system and the actual results checked against the predictions.

Note that only one good set of test data is needed to do all of the remainder of the optimization program.

The results of this work are now used to set up the controller.

9.4- Controller Adjustment - 'RCO'

The controller adjustment program 'RCO' permits the operator to have the computer set the controller board and the resonance compensation to the values coming from the automatic optimization program. Since three channels of controllers and resonance compensation boards were manufactured, it is necessary for the operator to set up the number of each board and relate it to a particular system so that the computer setup may fit the connections. Efforts are made in the program to prevent bumping of

the settings and causing system upset when a parameter is changed.

The program permits the operator to turn the reset off or on as well as change its setting. All of the settings are done to 12 bits within the ranges permitted.

The program interacts with the operator. The program also gives the settings already in the setup to the operator whenever it is queried.

Note how this program might be used to make fine adjustments in the controller settings to correct a frequency response and bring it into closer agreement with that needed for the particular test.

Each board used in the equipment provided under this contract has a number. The computer program 'RCO' programs that board and only that one so that the operator has complete control of the system and need not be concerned that the new settings will be entered anywhere else.

10.- The 'FRA' Program - Frequency Response Analyzer

10.1- General

The 'FRA' program operates the frequency response analyzer section of the equipments. The 'FRA' program is described in the sections below. First, the use of the 'FRA' program to set up the test signal in frequency, amplitude, and dc offset are presented. Then the manual setup of each channel of signal gain and dc reject are presented. The mode of the signal analysis which is to follow is set up including number of cycles to be integrated over, single run, continuous run, and sweep run modes. Finally, the method of programming the frequency response so as to record the results on the disc memory are given.

At each stage the operator's input to the program and the response as seen on the monitor (and or printer) are also given.

10.2- Test Signal Setup

10.2.1- Program Start

When the program is started or when the operator enters 'H' for help; the program causes the following listing to appear on the monitor:

Help, Freq, Amplitude, DC offset, Int no cycles
Gain, Exit, DC reject, Test '1 thru 99 Hz', List
Krun, Continuous, M-record on disc file

The operator moves to the function desired by the keyboard entry of the capital letter in the listing. For example, if the operator wishes the 'list', 'L' (or 'l') is depressed followed by depressing the carriage return key.

Using 'H' will cause this table to be written on the monitor whenever desired.

The frequency response analyzer is set to the following initial conditions by the startup of the program:

Frequency - 0.5 Hz	Amplitude of test signal - 0.0 volts
DC Offset of test signal - 0.0 volts	
Number of cycles integrated over - 1	
Sensitivity of each channel - 10.24 volts full scale	
DC Reject of each channel - 0.0 volts	

10.2.2- Test Signal Frequency

As shown on figure 10-1, the operator enters 'F' and then depresses the enter (carriage return) key. The computer responds with "Frequency in Hz from .01 thru 100.0 Hz." The operator then enters the desired operating frequency such as 36.2 Hz. This may be edited as desired until the desired value is on the screen. The operator then depresses the enter (carriage return) key. The computer causes the frequency to be programmed on the equipment and it responds on the monitor with, "Frequency = 36.200 Hz." If there were an error in the entry, such as an entry of 150.0 Hz, the computer would respond with "Incorrect entry - try again." The frequency would be left as before the incorrect entry was made.

The operator may continue to change frequency as desired or go on to other programming requirements.

10.2.3- Test Signal Amplitude

As shown in Figure 10-1, the operator enters 'A' and then depresses the enter (carriage return) key. The computer responds with "Amplitude = x.xxxx to 9.9999 volts peak" on the monitor. The operator then enters the desired peak amplitude, such as 4.5, and depresses the enter (carriage return) key. The computer responds with "Amplitude command is 4.5000 volts peak." If there was an error in the entry, such as an entry of 16.5 volts peak, the computer would respond with "Incorrect entry - try again." The test signal amplitude would be left at the value before the new entry was made.

The operator may continue to change signal amplitude or go on to other programming requirements.

10.2.4- Test Signal DC Offset

As shown in figure 10-1 the operator enters 'D' and then depresses the enter (carriage return) key. The computer responds with "DC Offset x.xxxx +- 9.999 volts." The operator then enters the desired dc offset in amplitude and sign, (when no sign is entered, a plus is assumed); such as, -3.45 and depresses the enter (carriage return) key. The computer responds with "DC Offset command is -3.4500 volts." If an incorrect entry is made, such as -11.5 volts; the computer responds with "Incorrect entry - try again." The dc offset on the test signal would be left at the value prior to the new entry.

The operator may continue to change the dc offset of the test signal or go on to other programming requirements.

10.3- Setup of Return Signal Amplifiers - Sensitivity and DC Reject

10.3.1 - Channel Sensitivity

The frequency response analyzer has channel sensitivities of 10.24 , 5.12, 2.56, 1.28, .64, .32, .16, .080, .040, .020, and .010 volts full scale. When the operator enters a desired volts full scale, the computer selects the range that is less sensitive than required but is closest to that desired.

If the operator wishes to set the sensitivity of each channel, the operator enters 'G' and depresses the enter (carriage return) key. The computer responds with :

"Present Values -Chan 1= 10.2400 ;Chan 2= 10.2400 volt FS"

"Desired Volt Full Scale 10.0 to .010 volts. "

Note that the present values displayed by the computer are those in use at the time the operator is doing the setting. The values shown are those set by the initial turn on of the 'FRA' program.

The operator enters the channel and value as:

"1 5.0" followed by depressing enter (carriage return). The computer responds with "Volts FS chan 1 is 5.1200 volt." The computer selected this full scale sensitivity as closest to that desired while being less sensitive (no overload will occur). The operator may now repeat the procedure for channel 2 or go on to other settings, etc.

Note that the program will change the channel sensitivity as the test proceeds as part of its AGC (automatic gain control) action to make each reading as accurate as needed to stay within its performance specification, and to stay out of saturation due to signal plus noise.

If an incorrect entry is made, such as 20.0 volts or the channel number is omitted, etc, the computer responds with " error in entry - try again" and leaves the sensitivity at its last setting.

This procedure is valuable at low frequencies in reducing the automatic gain setting time by anticipating where it should settle out.

10.3.2 - DC Reject in Both Channels

DC reject can be set to overcome the dc component of the signals being analyzed and permit the signal portion to be amplified sufficiently to permit accurate analysis. For example, if there are 4 volts of DC level, and 0.1 volt peak of signal, the channel sensitivity is more limited by the DC offset than by the signal level.

Note however that the program automatically adjusts the DC reject in each channel so that the signal portion may be amplified as much as needed for the desired accuracy. The dc reject setting need only be used by the operator in the initial setup for a new test as the normal operation of the system will maintain the desired dc reject setting.

The operator depresses 'J' to initiate the DC Reject setting followed by depressing enter (carriage return). The computer outputs "DC Reject - ch # 1 or # 2, x.xxxx +- 9.999 volts." The operator enters 1 5.6 followed by depressing enter (carriage return). The computer outputs to the monitor "SET DC REJECT to 5.6 volts in chan # 1."

The operator may repeat the procedure for channel # 2. Note that when a sign is not entered, plus is assumed.

10.4 - Number of Cycles for Integration

The key issue in the tradeoff between time and accuracy is the decision as to how many cycles of the test frequency to integrate over. In the low frequency ranges, this can make a great deal of difference as to how long the test will take. In the higher frequencies it makes very little difference. Thus, below one Hz, it is well to start with one cycle of the test frequency for the integration time, and above 10 Hz it is well to use 4 or 8 cycles of the test frequency to integrate over.

To set this parameter, the operator enters 'I' and depresses the enter (carriage return) key. The computer responds with "# cycles to be Integrated over - 1,2,4,8." The operator enters the desired value such as '4' and then depresses the enter (carriage return) key. The computer responds with a monitor entry of "Number of cycles = 4." If the entry is in error, such as entering '7', the computer responds with "Error - try again" and does not change the setting from its previous value.

Note that in the multipoint testing, the program sets the number of cycles to be integrated over. This saves the operator from forgetting to make this setting before a long run is started.

10.5- Review of the Settings - List

At any point in the setup of the frequency response analyzer, the operator may wish to review the present status of all of the settings. To accomplish this, the operator enters 'L' followed by depressing the enter (carriage return) key. The computer responds on the monitor with:

```
"Frequency setting is 0.500000  Amplitude is 0.0000 volts peak
DC Offset is  0.000 volts  Volt FS Chan1=10.240  Chan2=10.240
DC Reject Chan1=  0.000 Chan2=  0.000 Number of cycles integrated= 1"
```

The initial values are shown following startup of the program. The actual values at the time of requesting the list will be in the output.

This is a very simple way to check all of the parameters of the system prior to making changes or starting a new run.

10.6- Test Modes

10.6.1- Single Point - 'Krun"

The most frequently used mode is that of reading one point at the test conditions already set in the frequency response analyzer by the methods previously discussed in the earlier parts of section 10.

The operator enters 'K' and then depresses the enter (carriage return) key. This causes the following to happen:

The test signal is applied to the item under test.

Data is taken for each of the two channels to determine if the sensitivity and the dc reject are set in a reasonable fashion. This is done for one cycle of the test frequency. If a very large change is required in the sensitivity and the dc offset, a second one cycle run will automatically be made to bring the adjustments to settings that are as needed.

Then data is taken automatically for the number of cycles of the test signal as set by the operator and at the sensitivities and dc reject levels found in the earlier runs. This data is analyzed and the results are placed on the monitor in the following format:

```
"data being taken, run no 0, freq = 75.600
chan 1 , phase=- 37.66 , volts = 2.5884   ES = -1.0 +- 4.0
chan 2 , phase=- 38.76 , volts = 2.5476   ES = -1.1 +- 4.0
phase shift = 1.10   ratio 2/1 = -0.138 db  # cycles integrated=1
chan 1 Noise Volts = 0.0010 : Chan 2 Noise Volts = 0.0007 :"
```


The first line of the printout occurs as the run starts to let the operator know that a run is in progress and the frequency at which the run is being made. A run number is included for the case of multiple point runs.

The second line of the output is the result for channel number one compared to the reference. The phase in degrees and the amplitude in volts are given. Then another readout is given for 'ES' which is a measure of the signal plus noise. The DC component is followed by the peak value of the AC portion of the return signal to channel number one, at the A/D input.

The third line of the readout is a repeat for channel number two.

The fourth line of the printout computes the phase shift of channel 2 with respect to channel 1 and displays the result in degrees. Then it displays the ratio of channel 2 amplitude to channel 1 amplitude and gives the results in db. This db ratio of 2/1 includes all of the gain settings in the respective input amplifiers. Then the number of cycles of the test signal included in the result is presented.

Finally, another test is automatically done by the program when the test frequency is above 1.0 hz. This runs the test at the same sensitivity and dc offset as before, but with no test signal to the item under test. The result is a measure of the portion of the results which are due to noise in the system under test. If the noise measurement is large compared to the acceptable error in the results, the run should be redone with an increase in the setting for number of cycles of integration.

If there is a malfunction in the data taking process, an additional line will appear, following the first line with the statement "bad data" on the monitor. This means that the data taken did not correspond to half the points at 0° and half the points at 180° of the reference signal in succession. These results should be ignored and the run repeated.

If the data shows the amplitude of the signal to be less than 2% of full scale, the output will so state in the second line for channel 1 and the third line for channel 2. This appears on the monitor as: "less than .02 F. S. signal chan # 1 " (or #2).

10.6.2 - Continuous

In the continuous mode, the frequency response measurement is repeated again and again with a minimum output to the monitor (one line) of the overall results. This permits the operator to use the frequency response analyzer to achieve an adjustment of a system without having to restart the measurement cycle every time that a change is made in the system under adjustment. It can also be used to study the stability of the results with time and other operating conditions (such as varying oil pressure).

The program enters the continuous mode, when the operator enters 'C' and then depresses the enter (carriage return) key. The frequency response measurement is made as previously described under section 10.6.1 except that the output to the monitor is one line and a new run is started as soon as the previous run is completed. In addition, the noise measurement run is omitted. The readout is "DB= -21.53
Phase Shift = -135.67 at 13.0000 Hz."

Note that the first few runs may have to settle out at the proper gain and dc reject of both channels. Once this is accomplished, the runs will be of minimum and consistent time duration depending upon the test frequency and the number of cycles of integration.

The continuous mode can be aborted by the operator depressing any key. At the end of the run in progress at the time, the program will revert to its setup mode and will respond properly to the key that is entered.

10.6.3 - Test '1 thru 99 Hz'

There was a great deal of testing over the frequency range of 1 to 100 Hz. This operating mode was introduced to make the entire test complete, rapid and having a minimum of operator attention required to carry it out.

When the operator selects this mode by entering 'T' followed by depressing the enter (carriage return) key, the computer responds with a monitor output of " In Frequency test : 1 to 99 Hz in 42 steps" Then it outputs a second line to remind the operator that the disc recording function is on or off as " Disc Recording is ON " (or OFF). It would be usual for the 42-point test run to be recorded on the disc but it is not necessary to perform the run (the operator may elect to put the output on a printed output, etc.).

The program then causes two runs to be made (as in 'Krun' of section 10.6.1) at 1.0 hz. It outputs a line to the monitor of "Testing at 1.0 hz for correct results." Then it outputs all of the results of each of these runs. Then it outputs to the monitor "Enter 'C' to continue, 'E' to abort."

The operator studies the results of the first two runs and decides if everything is set up and working as was expected. If it is satisfactory the operator enters 'C'. If the operator is not satisfied and wishes to make changes before proceeding with the long test, 'E' is entered and the program returns to the setup condition, where the operator may make such changes as indicated before starting the multipoint test again.

If the operator elects to go ahead and enters 'C', the computer responds with "44 point test from 1 thru 99 Hz has started."

In this mode, the computer selects the number of cycles to be integrated over as 4 in the 1 thru 10 Hz range and as 8 in the 10 thru 100 Hz range.

The frequencies tested are:

1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 2.4, 2.8, 3.0, 3.4, 3.7, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 12.0, 14.0, 16.0, 18.0, 20.0, 24.0, 28.0, 30.0, 34.0, 37.0, 40.0, 45.0, 50.0, 55.0, 60.0, 65.0, 70.0, 75.0, 80.0, 90.0 Hz.

The computer program proceeds a point at a time to perform 42 frequency-response measurements. At the end of the first 21 measurements, a table of the results is output to the monitor which summarizes the results of the measurements as follows:

First, a line is output to the monitor that gives the test signal amplitude, the gain settings of each of the channels, and the number of cycles integrated over. Then a second line is output giving the headings of the columns that are to follow as "frequency : phase 1, 2 : phase shift , DB , : volts 1, volts 2." Then for each test point a listing is made of the test frequency, the phase of each channel with respect to the reference, the phase shift of channel 2 with respect to channel 1, the db ratio of channel 2/channel 1, and the volts of signal in channel 1 and channel 2.

This is followed immediately by a second listing which assists the operator and later those using the data in evaluating how valid

the data is. The heading line is "Frequency ES Output 1 2 ; Volts FS 1 2; Noise Level 1 2." Thus each line includes the test frequency, the signal level at the output of the input amplifiers, the volts full-scale sensitivity of each channel, and the noise level measurement at each channel. This data can be used to show if the measurement was made under reasonable conditions of signal to noise and under reasonable conditions of signal to total sensitivity.

Note that at the end of each run, the computer turns the test signal off. Thus, the item under test is only turned on for the time needed to settle and for the computer to take the necessary data. The time spent reducing the data and the time spent outputting the results do not have the item under test being driven by the test signal. This minimizes the wear and tear on the test item. The end of the test also has the test signal turned off. Thus, the operator may walk away from this test and yet have the test require a minimum of usage of the equipments.

If anywhere in the run, the operator decides to stop the run, the operator depresses the 'S' key. At the end of the frequency test point in progress, the computer prints out, "STOPPED - Abort or Continue?". If the operator enters an 'A', all of the files will be closed and the program will return to the test setup condition. This is the simplest way that the operator may limit the number of points say to the lowest portion of the frequency range. If the operator enters a 'C', the program will continue from the point where it left off. This may be done due to the need to examine some item of equipment before proceeding, etc.

If the operator enters any other character on the keyboard, the run will stop also at the end of the present test point. The message "Incorrect entry - Abort or Continue?" will appear on the monitor. The operator then has the same choices as above with the same set of consequences.

This program opens up the possibility of adding additional ranges and additional conditions under which many points are taken automatically.

10.7 - Recording on Disc

The operator may decide to record all of the data taken by the frequency response analyzer on the disc for a permanent record of the test results. The decision to record on disc also permits the obtaining of data automatically that can be used with the 'Mp' program to evaluate the needed gain, reset, and resonance compensation settings for the desired level of closed-loop performance.

To cause the program to record on disc, the operator enters 'M' followed by depressing the enter (carriage return) key. The computer responds on the monitor with " record name 8 characters max - e to exit." The operator now enters a name for the record which becomes the heading of the files which are prepared by the computer. If an 'e' is entered, the program returns to the setup condition and the operator may make such other decisions as needed.

After the operator enters the name of the disc file, the program responds with "opened files name.gen name.dat." If for any reason, the program was unable to open the files (such as the disc being full), the computer will output to the monitor "can't open name.gen" (or .dat) and will return to the setup condition.

If the files were successfully opened, the program then outputs to the monitor "comments - one line." The operator may now enter up to one entire line of comments which identifies the conditions under which the test was run. For example, the operator may enter the date, the load condition, the reset setting, and such other pertinent data as will identify the run for future study. These comments are echoed on the next line of the monitor and they become part of the name.gen file.

From then on as tests are done, all of the material that is shown on the monitor becomes a part of the name.gen file and the results of the 42point test becomes a part of the name.dat file as well.

The use of disc files to make a record of the testing with the frequency response analyzer in a systematic manner will greatly assist in reducing the future need for testing of the same system and will greatly enhance the value obtained from the use of the 'Mp' program.

11. The 'Mp' Program - Automatic Computer Solution of the Optimum Control System Parameter Adjustments

11.1- General

The 'Mp' program permits the study of the adjustment of the control system parameters starting with the open-loop frequency response as measured by the frequency response analyzer and placed on the disc in the name.dat file . The program permits the study of loop gain, resonance compensation, and reset. It also permits some study of integral compensation.

The program accomplishes its purpose one step at a time ; but with some insight into the theory of closed loop systems , each step can be built on leading to a complex but practical result that would be very difficult to impossible to find without the computer's assistance.

The parameters may be studied without tying up the item under test. Once its frequency response is known and measured, it need only be used again to confirm that the predictions made on the computer agree in fact with the end results using the parameters as predicted by the computer.

11.2 - Program Startup

When the program 'Mp' is started, it asks the operator for " Value of Reset in rpm ??". . The operator enters the value for the rpm at which the data to be studied was set. This is used by the computations in all that follows.

The computer then asks by way of the monitor for " file name?". . The operator enters the name of the .dat file that is to be studied. The computer opens this file and reads its data into the program arrays. If the file is not found on the disc, the reply "cannot open name.dat " is put on the monitor and the program returns to its starting point.

If the computer is successful in opening and reading the file , it then computes the closed loop frequency response of the system as measured. Then it finds the loop gain which will give a maximum output/ input vs frequency of 0 db (1.0) . The program uses this loop gain to compute the closed-loop response at all of the other test frequencies.

When this is completed, the computer outputs "closed loop adjusted for Mp=0 db, rpm = xx (value as given)."

Figure 11-1 is a printout of the exchange between the operator and the computer followed by the table of results as computed for the original system. Note the computer asks for the file name. The operator enters the file name. The computer reads the file and analyzes the data. It outputs the following characteristics of the closed loop system set for maximum output/input = 1.0 (Mp= 0 db):

Peak(in the closed loop response) at x.xx Hz
delta_gain = xx.xx db (change in open loop gain to achieve
Mp= 0 db).
Max LF DEV = ±xx.xx db (worst-case deviation of the closed-
loop response from 0 db below the resonant freq.)
-1 db BW x.xx Hz (frequency at which output/input is
down 1 db)
-20db at xx.xx Hz (frequency at which the output/input is
down 20 db)

These qualifiers assist the operator in deciding on whether adjusting loop gain by itself is sufficient to achieve the desired performance.

Then a listing occurs of the open-loop amplitude response as measured (OL amp) , and the closed-loop response as computed in amplitude and phase (CL amp 0amp) vs the frequency of each test point. The data is tabulated in two columns for ease in reading.

Then the computer prints out the menu of selections that the operator may do next.

11.3 - Adjustment of the Resonance Compensation

The operator enters a 'T' and enter (carriage return) to cause the program to study the adjustment of the resonance compensation. Fig 11-2 is the operator-computer exchange that follows this entry for the case shown in fig 11-1 . The computer outputs to the monitor 'in TRY', 'Bandwidth ?'. The operator decides upon the bandwidth that is desirable for the system with the resonance compensation present. Normally this is a lower value than that achieved with gain adjustment alone but one expects that the closed loop characteristics will be improved. The operator enters 4 and the computer responds with 'try for 4.00 Hz bandwidth'.

Second, the operator may cause the computer to try for a optimum adjustment at a lower value of damping ratio (DR). The operator enters 'C' and enter (carriage return). The program then takes the original data and tries for the desired adjustment of the closed loop system with a damping ratio of 1.75 as the starting value. There are instances where this is a valuable approach as the system responds better to the lower damping ratio.

Third the operator may want to know what effect a small change in the DR setting would have on the system. To find this out, the operator enters 'I' and enter (carriage return). The program computes the system response for the last damping ratio ± 0.1 and lists the results for study. This will show how sensitive the system is to the setting of the damping ratio of the resonance compensation.

If the computer fails to find a satisfactory adjustment of the resonance compensation after six tries, it prints out the results of the last try and leaves it to the operator to make the next decision as to what to do .

11.4 - Change Reset

The operator may elect to modify the original data as if there was a change in the value of the reset (RPM). This is done at the start of a study. The operator enters the 'Mp' program and enters the name of the file as discussed in Section 11.2. Then the operator enters an 'S' and enter (carriage return). The computer responds on the monitor with:

'Remove RESET	- type '1', RPM= ??'
' Add RESET	- type '2', RPM= ??'
' Change Reset	-type '3', RPM = ??'

The operator responds on the keyboard with '3 600' as shown in figure 11-3. Since the original system had a reset of 60 RPM , the computer now responds with 'Break Frequency = 0.159 Hz ' (the original) and 'Break Frequency = 1.592 ' (the new) value of the reset break frequency in Hz.

Then the program changes the open-loop data in two steps. It removes the effect of the original reset setting and enters the effect of the new reset setting. Then the program gives the closed-loop response of the

modified system. The listing includes all of the qualifiers as previously discussed as well as a listing of the open-loop amplitude ratio and phase shift vs frequency with a final column of the closed-loop response when the loop gain is set for $M_p = 0$ db. The operator may now compare this listing with the one for the original setting of reset and see what effect the reset has had upon the system. The operator may now also proceed with the optimization of the system with adjustment of the resonance compensation as in section 11.3. The program will treat the data with the new value of reset as the data that describes the system.

By this means the operator may explore the adjustment of the system for both the resonance compensation and the reset.

The operator may remove reset altogether using the '1' command. The operator may add reset to a system that does not already have it by using the '2' command.

The program causes a printout with the listing of the reset that is then present in the system. It must be stressed that the operator is responsible to check that the reset in the original data was that given to the computer.

11.5- The 'name.dat' File - Source & Modification

There are two methods of generating the 'name.dat' file that is the input data for the 'Mp' program. First is the automatic generation of this file when the frequency response analyzer is used with the disc recording turned on and the testing done automatically from 1 thru 99 hz. This provides 42 points from 1 thru 99 hz as has been previously discussed in section 10.6.3

Second is the use of the editor as supplied with the computer to start and make a file manually. This must follow the format for the other 'name.dat' files exactly for it to be read correctly by the 'Mp' program. This method is used whenever the data is obtained by single point testing or the data is obtained from other test procedures or methods.

A combination of these methods can also be used. The original file can be generated by the 1 thru 99 hz test.

The value of bandwidth entered by the operator must be one of the test frequency values. The program starts by trying a setting of resonant frequency (RF) = 35.00 Hz and a damping ratio (DR) = 2.00 . The computer output to the monitor shows that a bandwidth of 5.50 Hz was obtained with this setting of the resonance compensation and that it required a loop gain change of 10.52 db for an $M_p = 0$ db.

The program compares this result with that entered as the desired bandwidth of the closed-loop system (4.00 Hz) and decides to lower the frequency of the resonance compensation and try again. It does so and prints out the results as shown of a 5.00 Hz closed-loop bandwidth when the resonance compensation is set at RF + 25 Hz and DR = 2.00 .

The program again compares this result with the desired bandwidth and decides to try a lower setting of the resonance compensation RF. Each try involves a change in frequency of $\frac{1}{2}$ the last change. Thus, as the program first try is a 10 Hz change (from 35 to 25 Hz) , the next try is at RF = 20.00. When this is computed out, the results give a closed loop peak at 4.50 Hz. This result is within one test value of that desired and the maximum response at the desired bandwidth of 4.00 Hz is very close to 0 db . The program therefore, decides to settle for this result and tabulates the closed-loop results, as follows:

The first column is the frequency in Hz. The second column 'OL amp' is the amplitude response in db of the open-loop system as it originally was, and the third column is the closed-loop response of the system with the value of resonance compensation as determined above 'wRC'.

The qualifiers for the newly compensated system are also listed. They can be compared with those of the previous run for their improvement and as to whether the true performance has been obtained.

The operator now has several choices of how to further explore the effect of resonance compensation changes upon the system performance. First, the operator may repeat the above study using a different value of desired bandwidth of the closed loop system. 'T' is entered, and a value other than 4.00 Hz is used for the 'Bandwidth?' entry.

Then additional data may be added using the editor from results obtained from single frequency testing, etc. For example, the file shown in figure 11-2 has data added for the test frequencies of 0.1, 0.15, 0.20, 0.30, 0.40, 0.60, 0.80 Hz. This data was taken one frequency at a time and then appended to the 'p1-trial.dat' file. This made it possible to include the response at these low frequencies in the study.

There is no limit beyond the programs limit of 150 points to how many test points may be added to the 'name.dat' file so that more and more detailed analysis can be done of the results of the open-loop tests in predicting the closed-loop results. Of course, the program runs slower as the number of points increases.

In order to make the results more realistic, the program was modified to allow for values of M_p that exceed 0 db below 1.0 Hz. Looked at another way, the program adjusts for $M_p=0$ db above 1.0 Hz. This permits a much more meaningful study of the response at low frequencies (below 1.0 Hz) as reset is adjusted or as unusual closed-loop systems are analyzed.

11.6 - Integral Compensation

The operator now has the ability to use the 'Mp' program to study the effect of integral compensation upon the system response. This is presented in detail in Report # 21 of April 4, 1985.

The operator enters 'G' followed by enter (carriage return). The program responds on the monitor with 'First Break Frequency in Hz ??, Second Break Frequency ??' as shown in figure 11-4. The operator enters the desired break frequencies (.1 1 in the figure 11-4). The computer responds with 'Integral Compensation from 0.10 Hz to 1.00 Hz'.

The program then adds the integral compensation to the open-loop system and computes the closed-loop response for $M_p=0$ db. The results are given in one line of 'Peak at x.xx Hz ; delta gain = xx.xx db for $M_p = 0$ db'. In this case 2.80 Hz and 24.43 db. Then the data file is again listed and the reset value is given. Finally the listing is made of frequency, open-loop phase, open-loop amplitude and closed-loop amplitude response.

This data is used by the operator to decide whether the objectives have been met or whether there are other values to be tried.

11.7- Plotting the Results

The operator of the 'Mp' program may wish to use the results by plotting the open-loop data and seeing the closed-loop response for different gains. This establishes the sensitivity to gain change of the open-loop system and it shows what form of compensation change may improve the system response.

In this work, the Nichols chart in the form shown in figure 11-5 has been used. Figure 11-6 shows a simpler version that supplies most of the information required in this application and particularly useful in the early stages. The application of the chart of fig. 11-6 to the case presented in fig. 11-4 is given in fig. 11-7. It clearly shows what the program 'Mp' did in optimizing the loop gain for $M_p = 0$ db and it shows the gain sensitivity of the results.

It is recommended that the user of the 'Mp' program become familiar with the Nichols charts and uses them in their work of optimizing the system parameters.

12.- The 'RCO' Program - Computer Setup of the Controller and the Resonance Compensation for Three Channels

12.1-General

The 'RCO' program permits the operator to use the computer to set values of gain and reset into the controllers and resonant frequency and damping ratio into the resonance compensation boards. Each of these units is identified with a particular channel of operation by the board number for up to three channels of control.

This program does not set up the feedforward networks because they were specified as manual operation for this contract. Note also that there were no integral compensation boards provided with this contract in either the manual or computer controlled modes.

The operator must know, from the wiring of the computer controlled components in the system, which controller and which resonance compensation board went into each control system for the one, two, or three systems that may be in use. The computer actually addresses each board by its number, as given and described in the material below.

12.2- Program Startup

The operator enters 'RCO' followed by enter (carriage return). The program responds with a monitor output of "Number of Systems in Use 1, 2, 3?". The operator enters the number and depresses the enter key. The computer responds with "NUMBER OF SYSTEMS - x". This echoing of the operator's entries assures that the computer accepted the input which the operator meant to give it and permits the operator to make corrections if a bad entry is made.

The computer then reads in the data from the file 'setup.dat'. This includes the board number assignments to their respective systems and the recommended parameter settings from the previous work done on the systems.

A typical SETUP.DAT file is shown in figure 12.1.

To be certain that the operator is aware of the values read in, the computer outputs the following to the monitor:

'READINGS FROM DISC ARE:

System x , Controller x , RC x , Channel x

Read as RF = xx : DR = x.x : PB = xx : RPM = xxx'

with the values of the xs replaced by the actual values in the file.

This display repeats for up to three times depending upon the number of systems specified when the number of systems was requested.

The computer sets the systems in use to their minimum settings of PB = 100%, RPM = 6, and OFF, RF = 50 Hz and DR = 2.0. These are the settings least likely to be troublesome while waiting for the operator to decide what should occur next.

The computer then causes the following display on the monitor:

'ENTER PROVEN SETTINGS INTO SYSTEM 1,2,3 OR NO MORE 0'

This gives the operator the opportunity to make use of the data from the setup.dat file in any one or more of the systems or in none (by entering '0').

A complete exchange between the operator and the computer when operating 'RCO' is shown in figure 12-2. It shows what the computer outputs and what the operator inputs.

The operator elected to enter the proven settings into system 2 and then into system 1. The entered values from the setup.dat file are equal to the minimum settings as a coincidence of the starting of the system. In any real case they would be totally different.

The monitor shows the actual values entered in response to the operator's request that the proven values be entered into system 2 and then into system 1.

The reset is left off. This is to allow the operator to select the time after the oil is turned on for the reset to be turned on. It prevents windup of the reset and the very bad transient that would occur when the oil pressure was turned on.

12.3- The Menu

The computer now outputs the menu or choices that the operator may select or not in the continued operation of the 'RCO' program:

'manual change Resonance Compensation - 'R'
manual change PB - 'B' RESET(rpm) - 'M'
exit - 'E' : Display Present Values - 'D'
RESET - ON - OFF 'S' '

Each of these choices are discussed in the sections which follow.

12.4 - Turning Reset ON or OFF

The operator enters S followed by depressing the enter (carriage return) key. The computer responds on the monitor with 'SYSTEM # '1' , '2' , '3' ? Finished 0 '. The operator enters the channel that is to be changed. The computer responds on the monitor with ' SYSTEM # x has RESET xxx rpm with RESET xxx(ON or OFF). The xs are replaced by the system number just entered and the value of reset that is presently in that system and whether it is on or off. Then the computer displays a second line 'RESET ON - '1' ; RESET OFF - '0' ? '. The operator enters the 1 or the 0 and the computer causes the reset to go on or off as commanded in the system specified.

The computer will then repeat the cycle starting at the first line , until the operator enters a 0 indicating that the changes in the reset on and reset off are completed. The computer then puts out the menu again.

12.5 - Changing the Proportional Band (PB)

The operator enters B followed by enter (carriage return) key being depressed. The computer outputs the following to the monitor: 'SYSTEM # - pb - 1.0 to 100.0 % ? ? '.

The operator now enters the system number and the desired pb setting followed by enter (carriage return). The computer echoes these entries in the line to the monitor of 'SYSTEM # x to have xx.x pb' with the xs replaced by the entered values. The computer checks that the requested pb is from 1 to 100.0 and enters the value in the specified system controller board.

The operator may return to this setting again if testing at a different pb setting is desired either later on or at once.

12.6 - Changing the RESET (rpm)

The operator enters M and then enter (carriage return). The computer responds with the message to the monitor 'SYSTEM # , RESET RPM 6 TO 6000 : ON '1' OFF '0' ? ? '. The operator enters the three items with a space between them on one line , such as 1 35 0 and enter (carriage return). The computer responds to the entry with a line on the monitor of 'SYSTEM # 1 to have RPM =35 RESET OFF (for the above entries). The computer checks that the values are within range and then enters them into the correct controller board.

The operator may make further changes in the RPM of system 1 by again entering M and enter, or the operator may go on to other considerations.

12.7 - Changing the Resonance Compensation

The operator enters R and enter (carriage return). The computer responds with the message to the monitor of 'SYSTEM #, Break Frequency, Damping Ratio ? ?'. The operator enters the desired values with a space between and on one line such as 1 22.5 1.65 and enter (carriage return). The computer responds with System # 1 to have , Break Frequency = 22.5 , Damping = 1.65'(for the example given) . The computer checks that the commanded values are within range (Break Frequency between 5.0 and 50.0 Hz, and Damping Ratio between 0.5 and 2.0) . The values are then entered into the resonance compensation board for the specified channel.

The operator may make further changes in the resonance compensation settings next or at a later time as required by the work in progress.

12.8 - Display of Present Settings

At any time after the program is entered following the selection of the number of channels and the reading in of the setup.dat file , the operator may check on the present setup of all of the programmable equipment by entering D and enter (carriage return) for display of present values. The computer responds on the monitor with the following listing for each channel in use :

```
'System # x  uses CONT # x, RC # x , CHANNEL # x'  
'CONTROLLER set at xx PB , xxx rpm , and is xxx (On or Off)'  
'RC set at  xx.x Hz , and at x.x DR'
```

The xs are replaced by the values last entered into the respective control function, etc. This gives the operator a quick check on the system setups.

12.9 - Exit - 'E'

When the operator decides to leave this program and return to the operating system, the operator enters E and depresses the enter (carriage return) key. The settings in the controller and resonance compensation boards will remain unchanged. The setup.dat file will also remain unchanged.

The operator may have found improved settings for the controller and the resonance compensation for the system as a part of the work with the 'RCO' program. To include the new settings into the setup.dat file, the edit capabilities of MINCE are used to change the numbers recorded in that file. Then the new settings will be used by 'RCO' when it is again put into action for further work with this system. The setup.dat file is not automatically changed each time the operator uses it because the new settings may only reflect a particular use of the system and not the general use it is usually put to.

13. 'Dig-Dat' Program - Digital Data Taking Using the Frequency Response Equipments

13.1 - The Menu

The operator starts the digital data-taking program by entering its name 'dig_dat' followed by enter (carriage return). The computer reads the program from the disc, and outputs the menu below. The menu may also be obtained at any point in performing the program by entering H followed by enter (carriage return).

The menu as it appears on the monitor is:

```
' Help, Samples per second, alias Filter, Amp  
  Take data, # of Points, Dc offset ,Record on disc  
  Gain, Exit, dc reject, List , analyze '
```

The letter that is capitalized in each item is the key to enter the item if followed by depressing the enter (carriage return) key.

The operator must now set up the conditions under which the test data is to be digitized.

13.2 - Samples Per Second

The operator enters S followed by depressing the enter key. The computer responds on the monitor with 'Samples per second 6,400 per channel per sec full scale'.

The operator enters the desired samples per second. The decision as to how many samples per second to specify is a compromise between a high sampling rate which limits the time covered by a given number of samples, and a low rate that doesn't correctly define the waveshape. A good rule to follow might be: If the signal to be digitized has significant components out to a frequency 'f1' Hz, then use a minimum of $(64 \times f1)$ samples per second as the sampling rate.

If the entry is greater than 1 sample per second and less than 6400 samples per second, the program will automatically set the computer to that sampling rate.

In terms of the frequency response analyzer, the computer causes the signal generator frequency to be the sampling rate divided by 64.

13.3 - Alias Filter Setup

The operator is referred to Section 2.3.4 for a discussion of the need for and design of the alias filter.

To set the alias filter, the operator enters F followed by depressing the enter (carriage return) key. The computer responds on the monitor with 'Alias set at 100x Samples/sec' and 'Set to 100x Sampling Freq -'0' to 1000x - '1' ?'.

In other words, the operator has two selections. The alias filter may be set close to the sampling rate as in the use of the frequency response analyzer of 100x the sampling rate, or it may be set further away by the use of 1000x the sampling rate. These are the only two choices given the operator.

After the operator enters the 0 or the 1, the computer responds on the monitor with 'Now set at x100 ' or 'Now set at x1000' depending upon the entry.

The computer sets up the alias filter automatically to agree with the sampling rate and the above selection. Anytime that the sampling rate is changed, the alias filter will follow it in the ratio given by this entry.

13.4 - # of Points Setup

The operator initiates the decision as to how many points to take by entering P followed by enter (carriage return). The computer responds on the monitor with 'Number of Points in Thousands 1 thru 7 ?'. The operator enters the number 1 thru 7 depending upon how many points are desired. This is equivalent to the length of the data sample to be digitized. For example, if the sampling rate is 200 points per second, 2,000 points corresponds to 10 seconds of actual run time that are being sampled.

The computer responds on the monitor with 'Number of points = x000', with x being the operator entered number of thousands. This value is set in the computer at the point where the decision is made to stop taking points.

13.5 - List of the Settings

Entering L and depressing the enter (carriage return) key causes the program to output a complete listing of the settings to the monitor. The monitor will show the following:

```
'Samples/second = xxxx      : Number of Samples  xxxx
Full Scale Volts chan 1  x.xxx , chan 2 x.xxx
Alias Filter se t 100 (or 1000)x sampling frequency
DC Reject Chan 1= x.xxx   : Chan 2 = x.xxx '
```

with the xs replaced by the actual values now in use by the program. At each stage in the setup the operator should consult this listing to be certain that the test system is properly setup.

13.6- Channel Sensitivity and DC Reject

The setting of channel sensitivity (gain) and DC reject follow the same procedure previously described for the frequency response analyzer in Sections 10.3.1 & 10.3.2 respectively. The operator must remember that the digital data taking program has no gain change or dc reject adjustment as apart of the run time operation. It is entirely up to the operator to set these adjustments. Fortunately there is a relatively simple method to do this.

The front panel of the individual input amplifier units have a test point marked 'OUT' as shown in figure 2-10. This is the output of the input amplifier and alias filter. It can be examined on an oscilloscope . The sensitivity of that channel and the DC reject should be adjsuted to use as much of the ± 10.0 volt range as is reasonable for the input being studied.

Of course, if the range of the input signal is known in volts, the dc reject level desired and the sensitivity can be computed and then set into the respective channel. For example, if the signal is going from +1 to +5 volts, the DC reject is set at +3.0 volts, and the sensitivity to 2.56 volts full scale. This will give a $(\pm 2.0/2.56)(10.0) = \pm 7.8$ volt swing at the output.

13.7 - Recording the Data on Disc

At the very start of the program the operator is asked by the computer by a display on the monitor of 'Record NAME 12 characters max - xxx.xxx - e to EXIT ' to name the recording to be made on disc. Once the operator enters the name, the computer responds with 'Opened file xxx.xxx ' as called for by the operator. If the operator entered an E, the program is exited.

If the file was opened , the computer next requests a line of comment as follows: 'Comments - one line ' on the monitor. The operator enters one line of comments to identify the conditions under which the data is being taken such as date, time, type run, system , or code number of the run, etc. The line of comments is entered into the file and is repeated on the monitor as 'Comments : -' followed by the line of comments as entered by the operator.

The data taken by the program will not be recorded on the disc unless the operator commands it to be recorded by entering R followed by enter (carriage return). The computer displays on the monitor

' Disc record will be made of next set of data
 unless you enter 'N' or 'n' '

The operator now enters N if no recording is desired , or any other key to obtain recording. If N is not entered, the computer responds with ' Disc recording will be made ' . If N is entered, the computer responds with ' No recording will be made on disc' .

13.8 - Taking Data -

To take data, the operator enters T followed by enter (carriage return) and the computer responds on the monitor with 'data being taken'. When the data taking is completed, the computer outputs ' data taking completed' to the monitor.

The computer converts the data as taken to useful form and then outputs to the monitor 'Convert completed '. If the data is being recorded on disc, the computer also outputs 'Disc record completed ' to the monitor. Thus the operator is kept aware of what stage the data taking is in at all times.

13.9 - Data Analysis

To analyze the data that has been taken, the operator enters Z followed by enter (carriage return). Several decisions have to be made before the analysis starts. To accomplish them, the computer puts the following on the monitor:

```
'rep-op on test- output results only - one delay - - '0'      '  
'display of all tables and values - - - - - '1'      '  
'display of all tables - every tenth value - - - - - '2'      '  
'display of first thousand points - all values -- - - '3'      '  
'display of every tenth point - first thousand points '4'      '
```

If the operator selects the first case '0' , the computer establishes the delay by asking the operator on the monitor 'Delay - ? - 0 to 30 '. The operator enters the desired delay and enter (carriage return).

An explanation of the effect of these choices is as follows: When the program is taking several thousand points , the listing of the results and the doing of the analysis of all of the points may take too long and spread out the results over too much paper. These choices permit seeing the essentials of the results without taking as much time and without taking as much room on the output device.

The '0' mode displays only the output results for a single delay. It permits the operator to change settings within the control system and to rapidly see how that effects the error (peak and average) between the input and output for the delay chosen. This can be used to optimize several systems for the same delay giving them nearly equal dynamic performance.

The '1' mode provides all of the tables and values in the outputs. No shortcut is taken.

The '2' mode limits the output to every tenth value of input. This if 1,000 points were taken, the output would be shown for every tenth point.

The '3' mode displays all of the results for the first thousand points. The '4' mode displays the results for every tenth point of the first first thousand points taken.

Note that in all of the above cases, all of the data is analyzed and the results are based upon the analysis of all of the data. Only the final output is limited so that it may be examined carefully.

The analysis process consists of the following steps:

First, the original data for the two channels is displayed to the scale factors given by the operator.

It is assumed that the two channels of data represent an input and output of a system,, or the outputs of two systems and that the comparison of the two channels has a physical significance.

Second, the mean value of the signal level in each channel is computed and displayed.

Third, the levels at each point have the mean value subtracted, and the new levels or the dynamic response is displayed.

Then an error is computed as the difference between channel 1 and channel 2 at each point in time . The error function is displayed as called for by the operator in the initial setup.

Then the process of computing the error for progressively larger time delays between input and output is is started. The input (channel 1) is is delayed by one time period, and a new error function is computed for channel 2 with respect to channel 1. The error is qualified as to a maximum positive value and a maximum negative value, and as to a total positive value and a total negative value (the total is non-dimensionalized by dividing by the total number of points). Finally, the total error is expressed as a percentage and is referred to as the Average + or - error. For example a value of +365 would imply an average plus error of 3.65 units.

These characteristics of the error are printed out for each value of the delay. The procedure then repeats for the next larger delay.

This will continue for up to 30 delays , unless a minimum is reached in the maximum positive error and then exceeded by two to one.

The error function of the optimum delay is then displayed.

Now the computation looks for a scale factor that would correct for the amplitude difference in channel 1 with respect to channel 2. The scale factor is printed out and the delay computation as described above is repeated for the newly scaled data.

13.10- Examples of the Application of the Digital Data-Taking Program

Figure 13-1 shows the first printout of the program run on one of the systems in the Structures Laboratory. Note that all of the data is expressed as 4095 being +10 volts, 2048 being zero volts and 0000 being -10 volts.

The printout starts with the selection of mode '4' which displays every tenth point of the first thousand values.

The source file is operator selected as ch6-dta.dat. The destination file for the results is 'try'.

The line of comments tells that the test was run on channel 6, on the afternoon of Dec. 7, and that the system was set up with pb = 70%, resonance compensation set at 35 hz, and a damping ratio of 2. It also indicates that the recording was done at 200 samples per second with the alias filter set at 100x the sampling frequency. The system is being run at 20 cycles per minute.

Then there is a listing of the original data with the point number followed by five readings from channel 1 followed by the corresponding five readings from channel 2.

For example, point number 520 is 1205 for chan 1 and is 1223 for chan 2.

Then the peak and the minimum value of each channel is given along with the delta value (peak minus the minimum), and the point where it occurred. Then the mean value for each channel is given.

Then the mean value is subtracted from each point and the results are printed out for all of the points and for both channels. Note that this includes plus and minus excursions around the mean.

Fig. 13-2 continues the output. The error function between channel 2 and channel 1 is now listed for each point.

The maximum plus error is noted and the point at which it occurred.

The maximum minus error is noted and the point where it occurred.

Now the delay of channel 1 with respect to channel 2 is entered for a delay of one time unit, then two time units, etc. At each value of delay new values of average + error, peak plus error, average minus error and peak minus error are determined and listed.

Consider delay = 8.. This means that channel 1 has been delayed by 8 units of time with respect to channel 2 or by $8/200 = 40$ msec. At this value . The average plus error is 5.89 units , The peak plus error is 27. The average minus error is 5.57 units and the peak minus error is -25.

The run stopped at a delay of 17 because the peak plus error was greater than twice the minimum found at a delay of 7.

The error table for the optimum delay is printed out for each point. Then the location of and the value of the peak + error and the peak minus error are printed out.

A scale factor is computed and printed out which is the ratio of the amplitude of each channel to each other.

Fig 13-3 now shows the continuing data reduction . The scale faactor is applied to channel 2 and the resulting dynamic response of the two channels is printed out at each point.

Then the delay procedure is carried out for the new data. Again the minimum is determined. This time it occurs at a delay of 6 units. The computation continues until a delay of 12 units at which time the error has more than doubled.

The optimum error function is listed.

Then a final effort to find the optimum delay is made by computing it for a delay of 6.5 units and for 5.5 units delay. Each point is linearly interpolated from its value one unit in time behind the present value and one unit in time ahead of the present delay time. The result is to find that at a delay of 6.5 units there is a lower value for the peak plus error and for the other error qualifiers. This is between the two values of delay that produced equal peak plus errors.

Note that the 6.5 unit delay is equivalent to a time delay of 32.5 milliseconds . This is a realistic value for operation at 20 rpm on these systems.

14- Conclusions and Recommendations

14.1 - Conclusions

As a result of the work done under this contract, we have shown that a considerable performance improvement in the dynamic response of the electro-hydraulic control systems used by the Structures Laboratory can be achieved by augmenting the compensation available to the operator in the electronic controller.

In particular, we have shown that the resonance compensation with adjustable frequency setting and adjustable damping ratio permit improved system performance when faced with the limitations imposed by structural and electro-hydraulic system resonances .

In addition, we have shown that those systems that have lost some or all of their low frequency integration, can be greatly improved by the use of integral compensation.

Because of the complex nature of the problem of adjusting a multi-function controller, we have shown how the computer can be used to assist in finding the optimum adjustments. This starts with the computer and our specially developed circuitry making a complete open-loop measurement of the frequency response of the system to be optimized. The computer and the operator working together then find the best adjustment of loop gain, reset, resonance compensation and integral compensation. While this procedure has not become completely automatic, we have taken it a long way so that in the hands of a knowledgeable engineer , it can arrive at a good system adjustment in a broad range of applications. The adjustment is found without further running of the system.

We have provided three channels of resonance compensation and controller boards that are both manually adjustable and computer adjustable with great precision and repeatability.

We have provided three channels of feedforward circuitry which is manually adjustable and provides a unique capability for correcting of deficiencies in the closed-loop response that cannot be corrected within the loop. This circuit also permits the matching of the dynamic performance of several control systems that are to operate together.

We have designed the integral compensation circuits that are precisely adjustable. These have been implemented temporarily on the feedforward boards.

We have provided interface boards that give the computers direct control over the frequency response measuring equipments and the controller and resonance compensation functions.

We have provided a complete two-channel frequency response analyzer which performs the precise measurements of amplitude ratio and phase shift despite high noise levels and harmonic content of the signals to be analyzed (permitting the testing to be done at low amplitudes so as not to cause damage to the structure). The frequency response analyzer is a combination of analog and digital technology that minimizes the hardware, makes maximum use of the computer and provides very high accuracy and repeatability of the results.

We have applied the technology, developed under this contract, extensively under actual laboratory conditions; first, to an experimental test setup and then to a wing fuel tank test setup. Thus the circuitry and the programs have undergone a steady upgrading under realistic conditions so that what has been supplied is immediately applicable to the work being done at the Structures Test Laboratory.

We have provided software for the operation of the frequency response analyzer, for the system optimization studies and for the use of the computer in making adjustments of reset, gain and the resonance compensation in up to three channels.

We have attempted to give the system an on-line mode for use in studying the systems operation while in use without injecting any test signals with a view toward on-line adaptive control capability. This has been done using the hardware already developed for the frequency response measurements. This has been referred to as digital data taking and data reduction. It shows great promise for automatic monitoring of system performance, and adjustment of system parameters or program speed to hold the performance within the desired limits.

The digital data-taking approach has also been shown to offer a

performance study based upon an equivalent system delay. Thus if the system is assigned an equivalent delay (as can be determined from one of the signal analysis procedures included in this program), then error is shown comparing the output with the input delayed by the equivalent system delay. This provides a true picture of how well the program is being followed and being reproduced. It should permit higher program speeds and thus less time per test.

14.2 - Recommendations for Further Work

There is much more that could be done to make the setup and adjustment of the control systems more automatic and to obtain even more dynamic response to permit even faster running of the fatigue tests.

First, it is necessary to study the effect of interaction of the control systems on each other and on the optimum adjustments. We have been able to greatly reduce some of the interaction with the use of the resonance compensation, but there is much more to do so that the computer recommendations match the performance actually obtained.

Second, complete controllers that are computer adjustable in all of their functions should be designed and built. This would greatly speed up the adjustment procedure and would give experience in the advantages of this equipment under full time use.

Third, the on-line digital data taking procedures should be advanced so that they can be used for monitoring shut-down conditions as well as doing error signal evaluation (using the equivalent delay) to do on-line system adjustments and program speed adjustment. This would be a true on-line adaptive control technology.

Fourth the frequency response measurement procedure should be made more automatic, and still further reduce the operator attention required to properly characterize the control system under study.

Fifth, the use of the feedforward capability should be studied in a multi-loop system to evaluate the improved performance that results from its use. This should include computer optimization of the settings and computer adjustment as well of the feedforward circuit.

All of this would give us one more step toward the day when the full capability of the loading systems would be achieved rapidly and nearly automatically and nearly all of the applications at the laboratory.

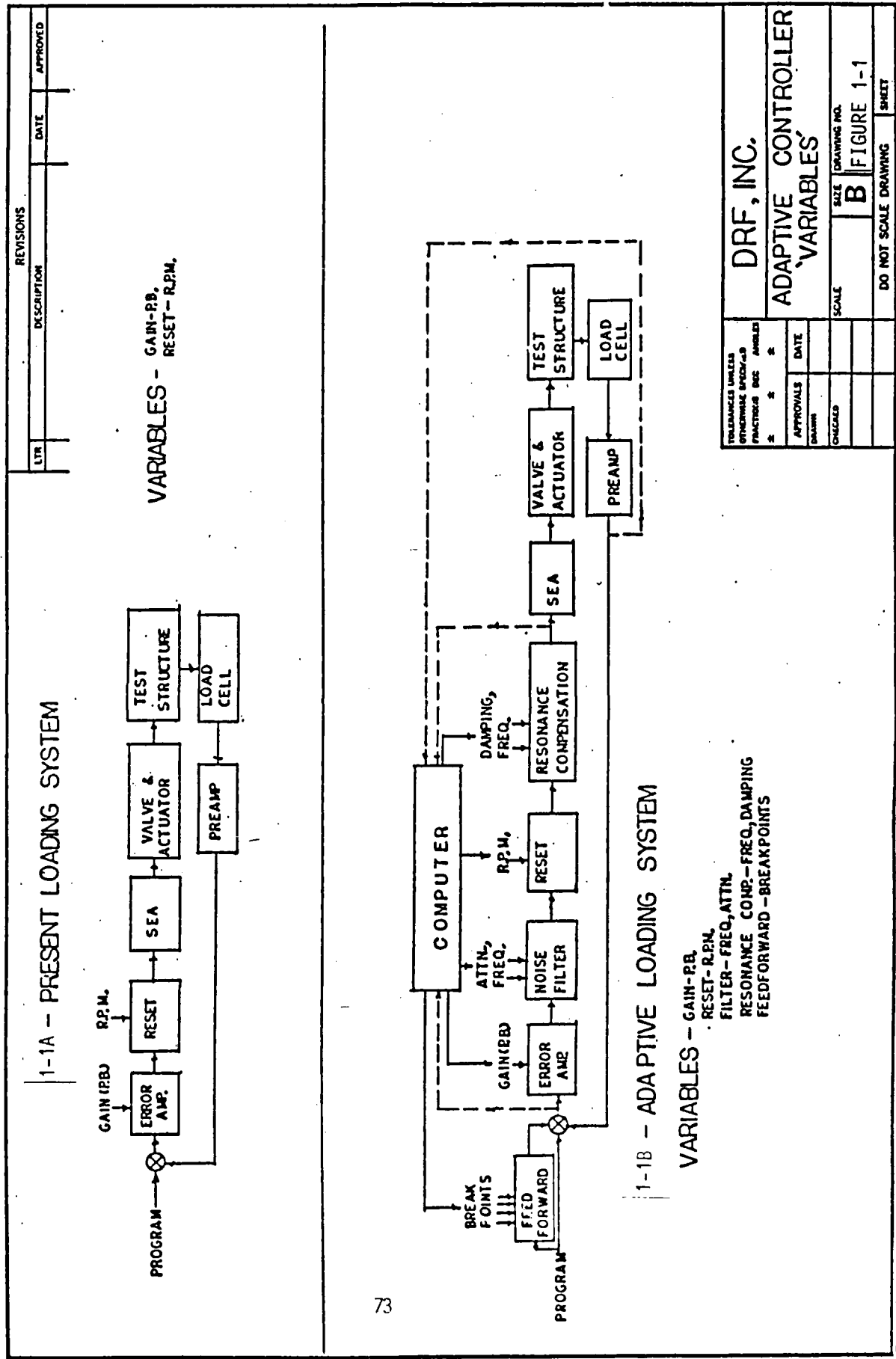


Figure 1-1. Adaptive Controller Variables

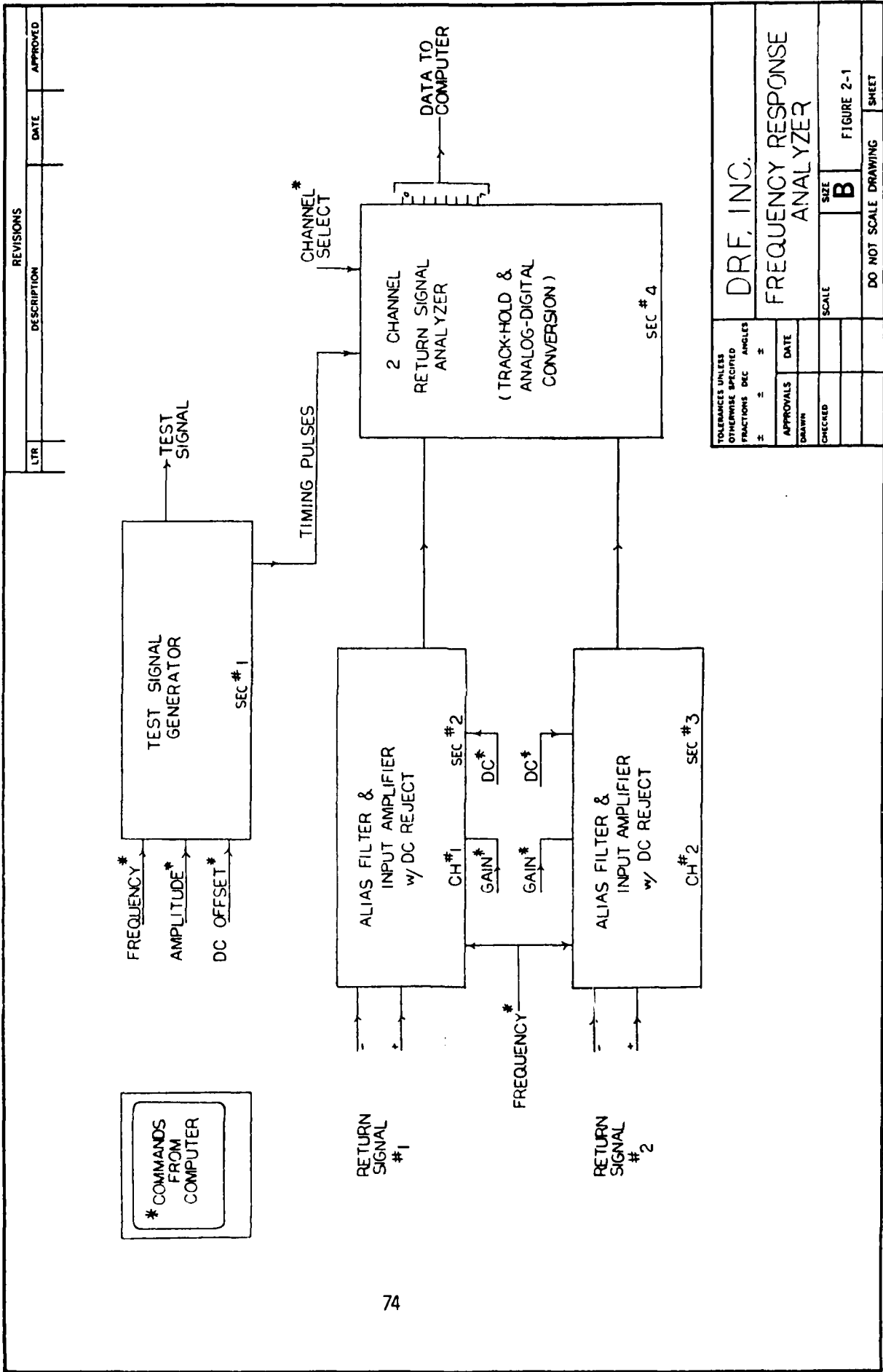


Figure 2-1. Frequency Response Analyzer

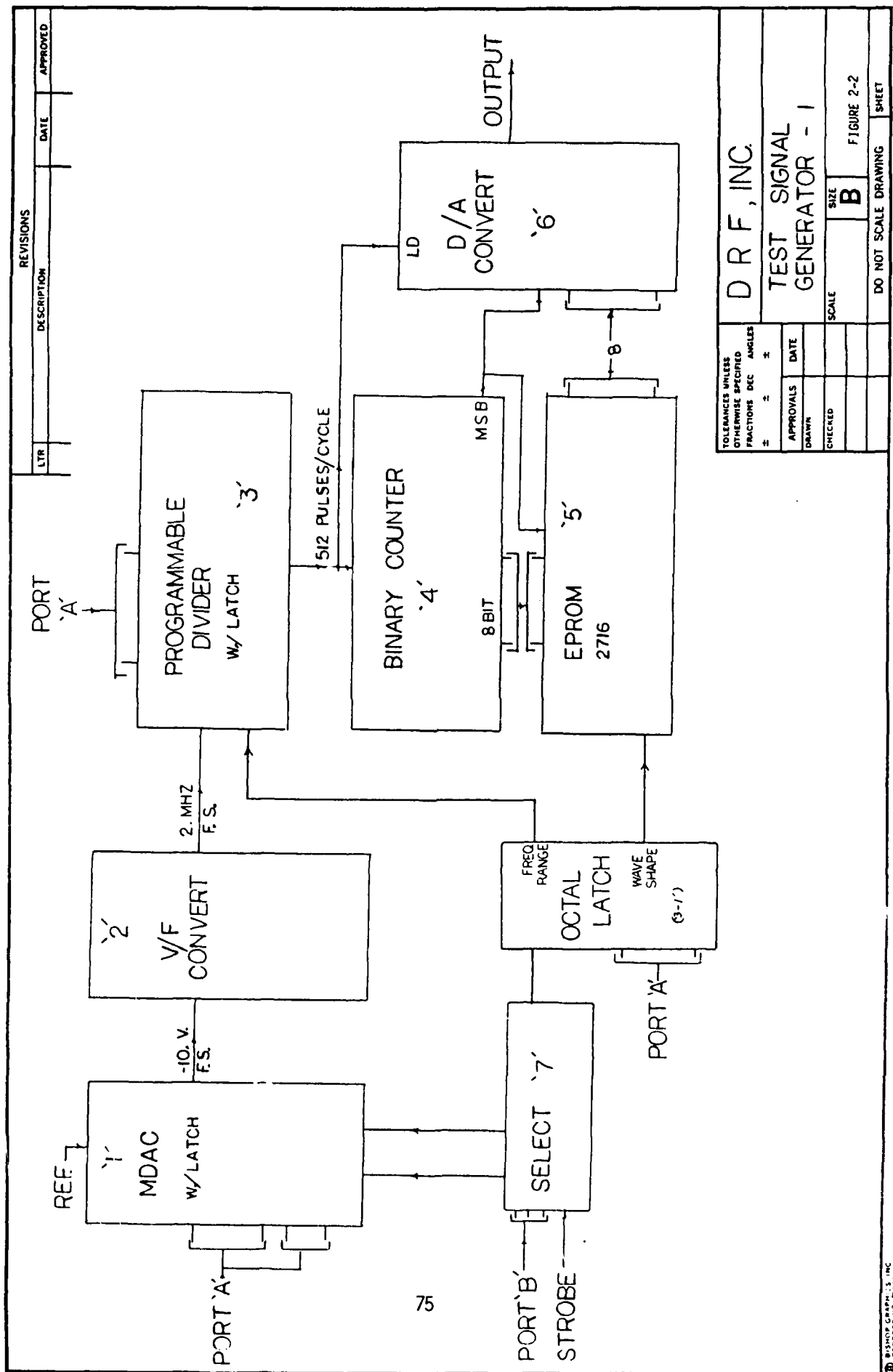


Figure 2-2. Test Signal Generator

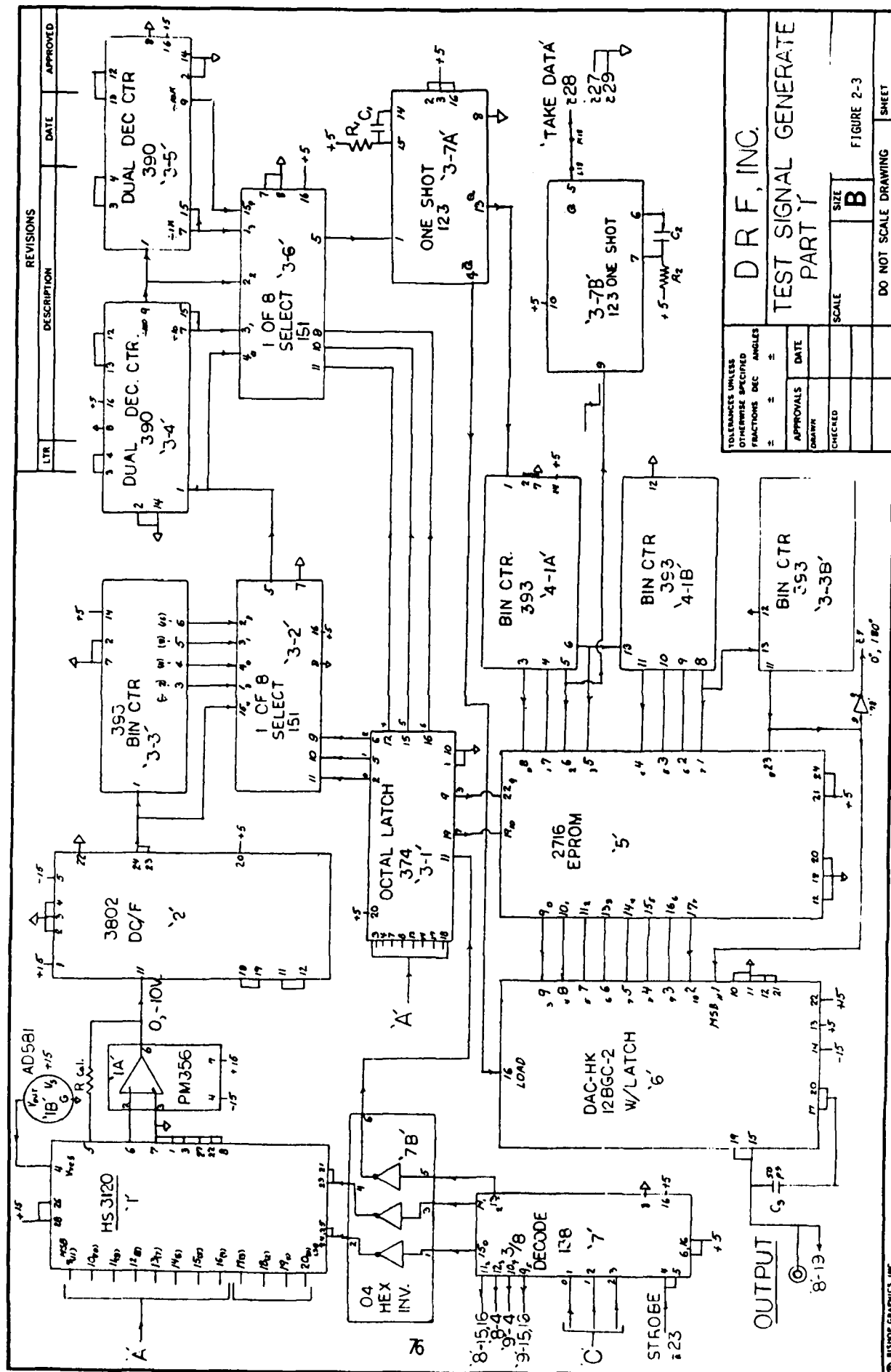
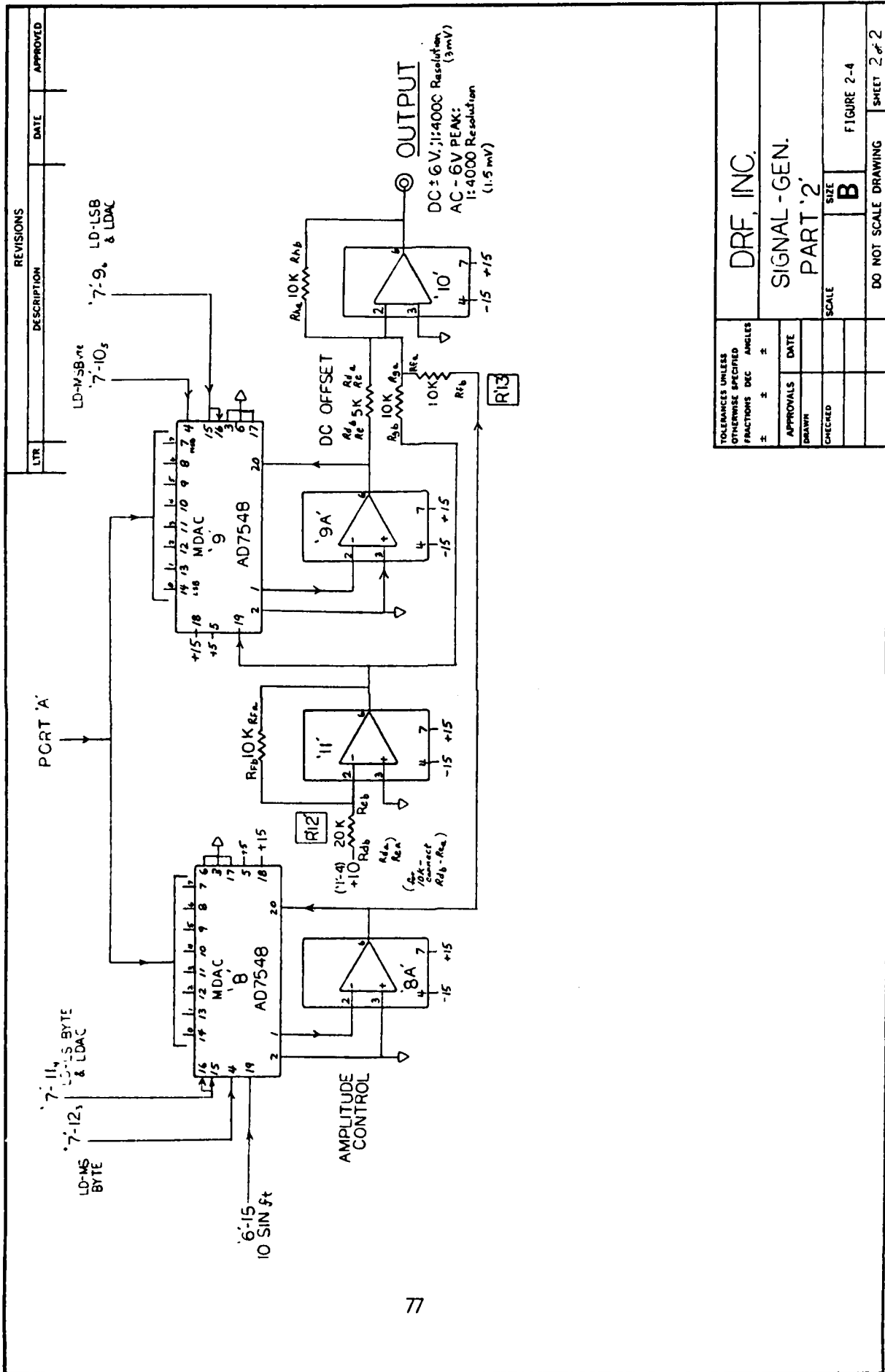


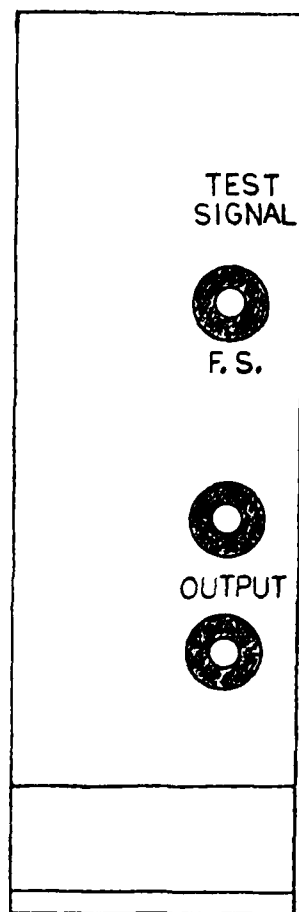
Figure 2-3. Test Signal Generate



TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES	
±	±	±	±
APPROVALS		DATE	
DRAWN			
CHECKED			
SCALE		SIZE	
		B	
DO NOT SCALE DRAWING		FIGURE 2-4	
		SHEET 2 of 2	

DRF, INC.
SIGNAL-GEN.
PART '2'

Figure 2-4. Signal - Gen.



TEST SIGNAL GENERATOR
FRONT PANEL

FIGURE 2-5

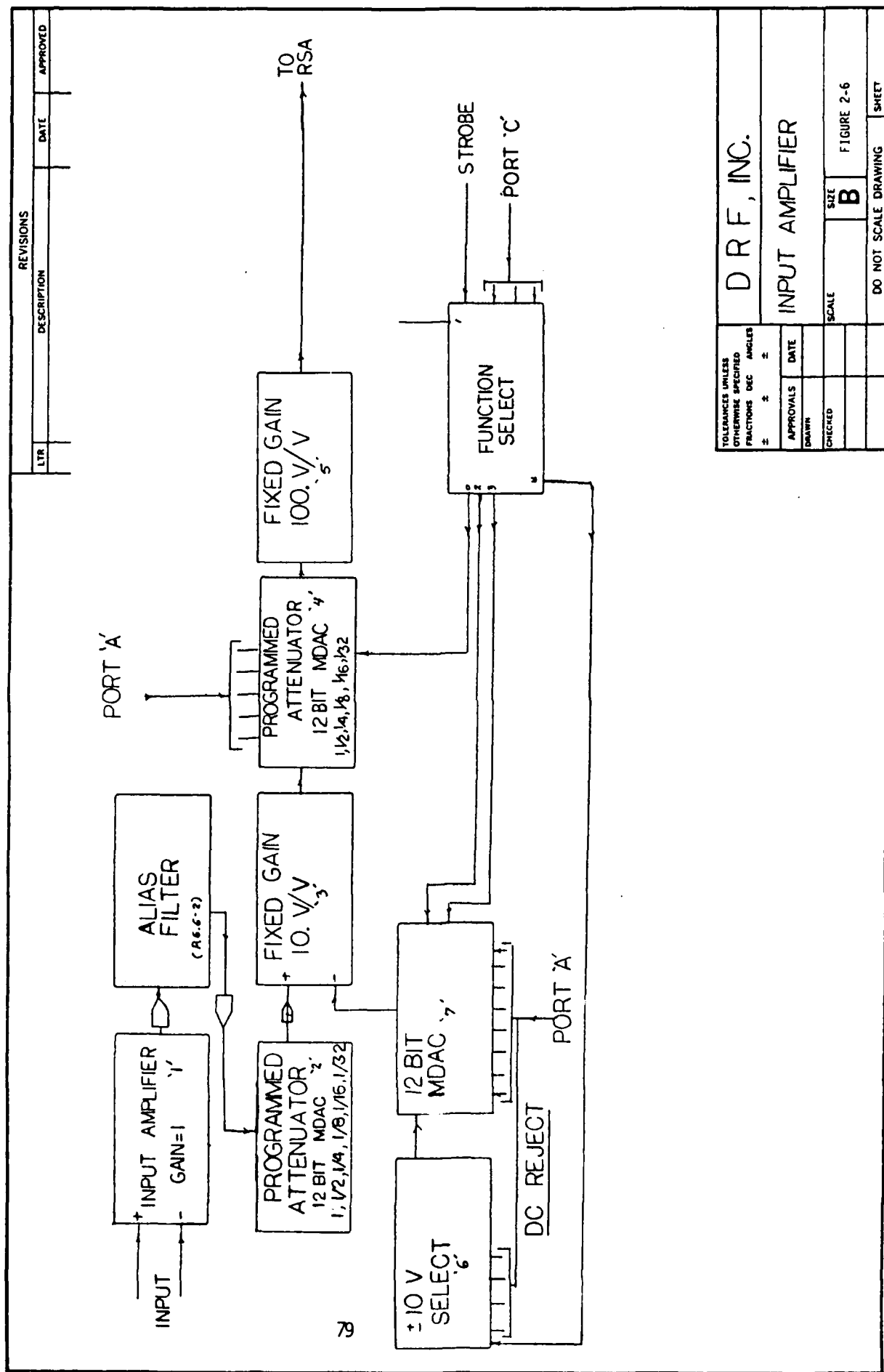


Figure 2-6. Input Amplifier

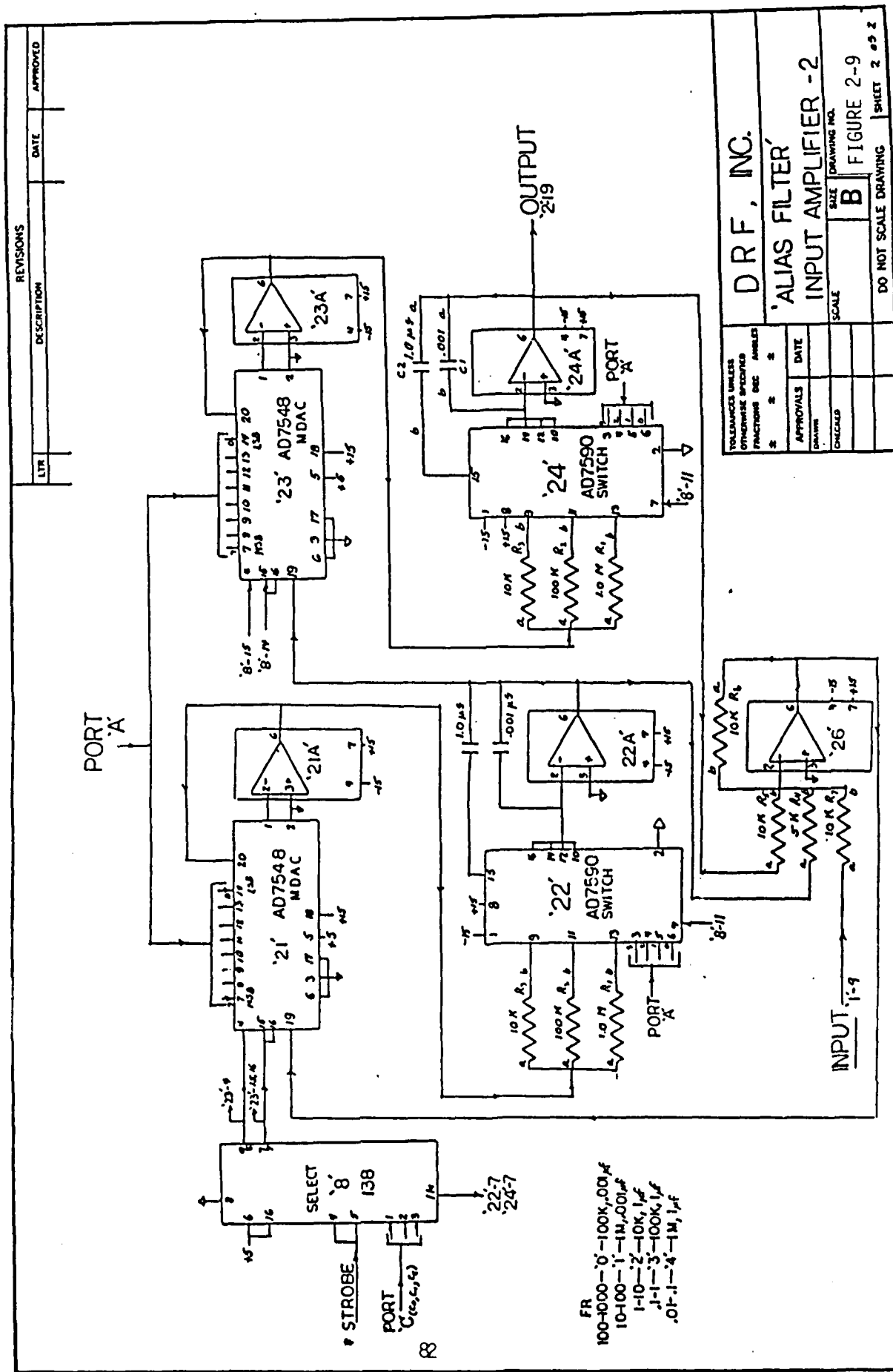


Figure 2-9. 'Alias Filter' Input Amplifier

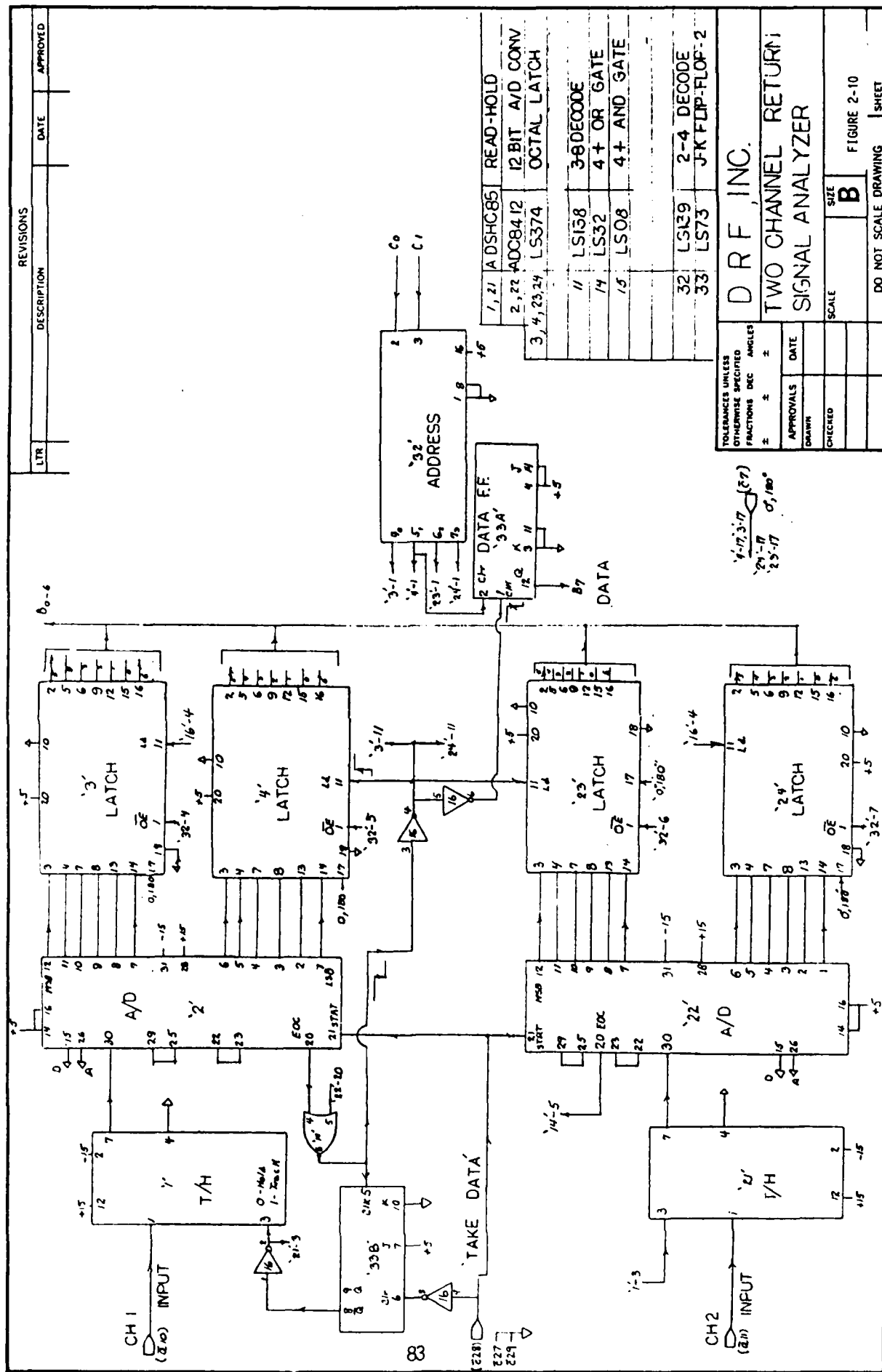


Figure 2-10. Two Channel Return Signal Analyzer

3/7/84

+20 - +90°

+10 -

0 -

-10 -

-20 -

-30 -

Phase

-90°

-30 -

-40 - -180°

0.1 - .2

.4 .6 .8 1.0

2 4 6 8 10.0

20

40

60

80

100

Frequency → Hz

Channel #6
Closed Loop

FIG 9.3.1

FIGURE 3-1

Figure 3-1. Channel #6 Closed Loop

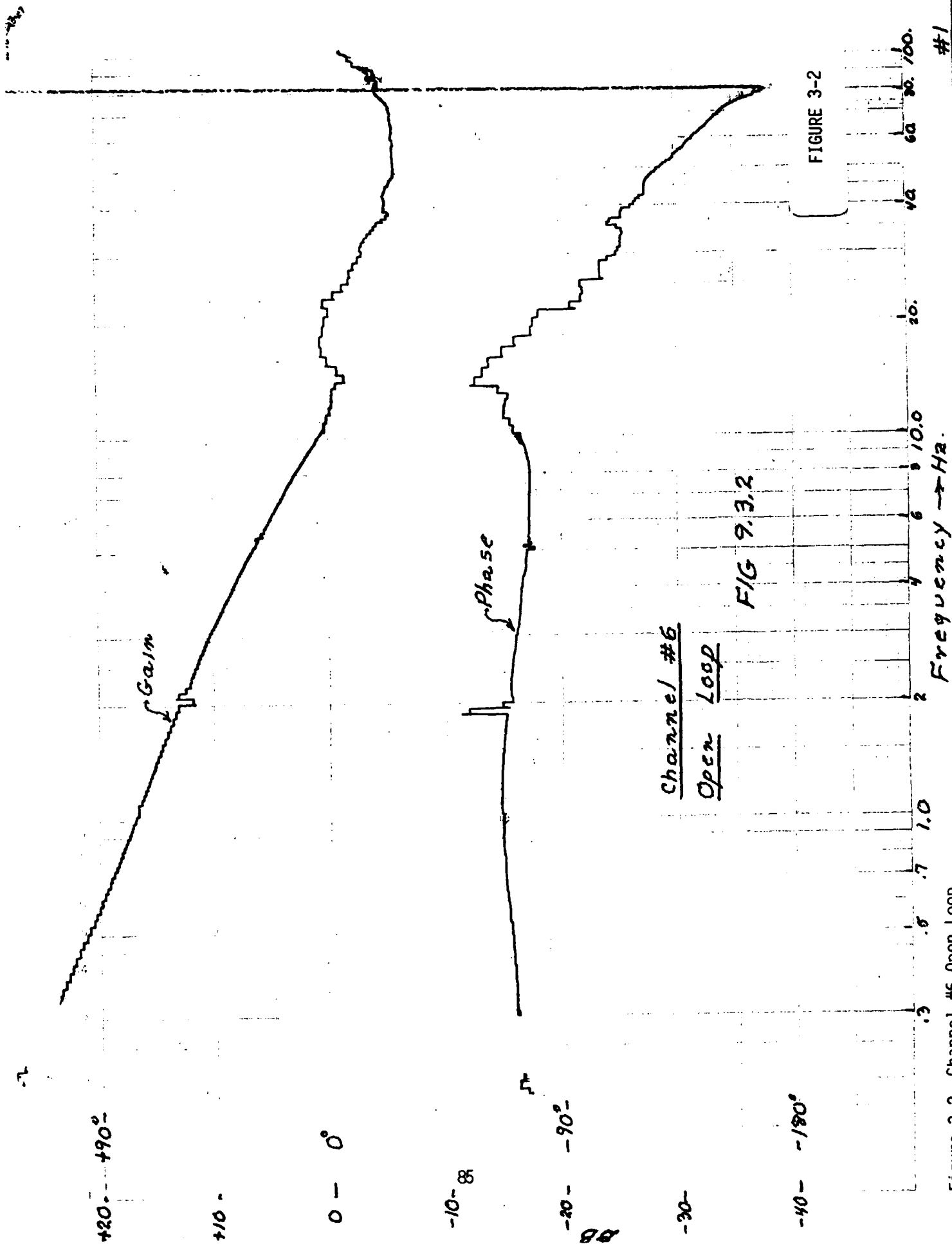


Figure 3-2. Channel #6 Open Loop

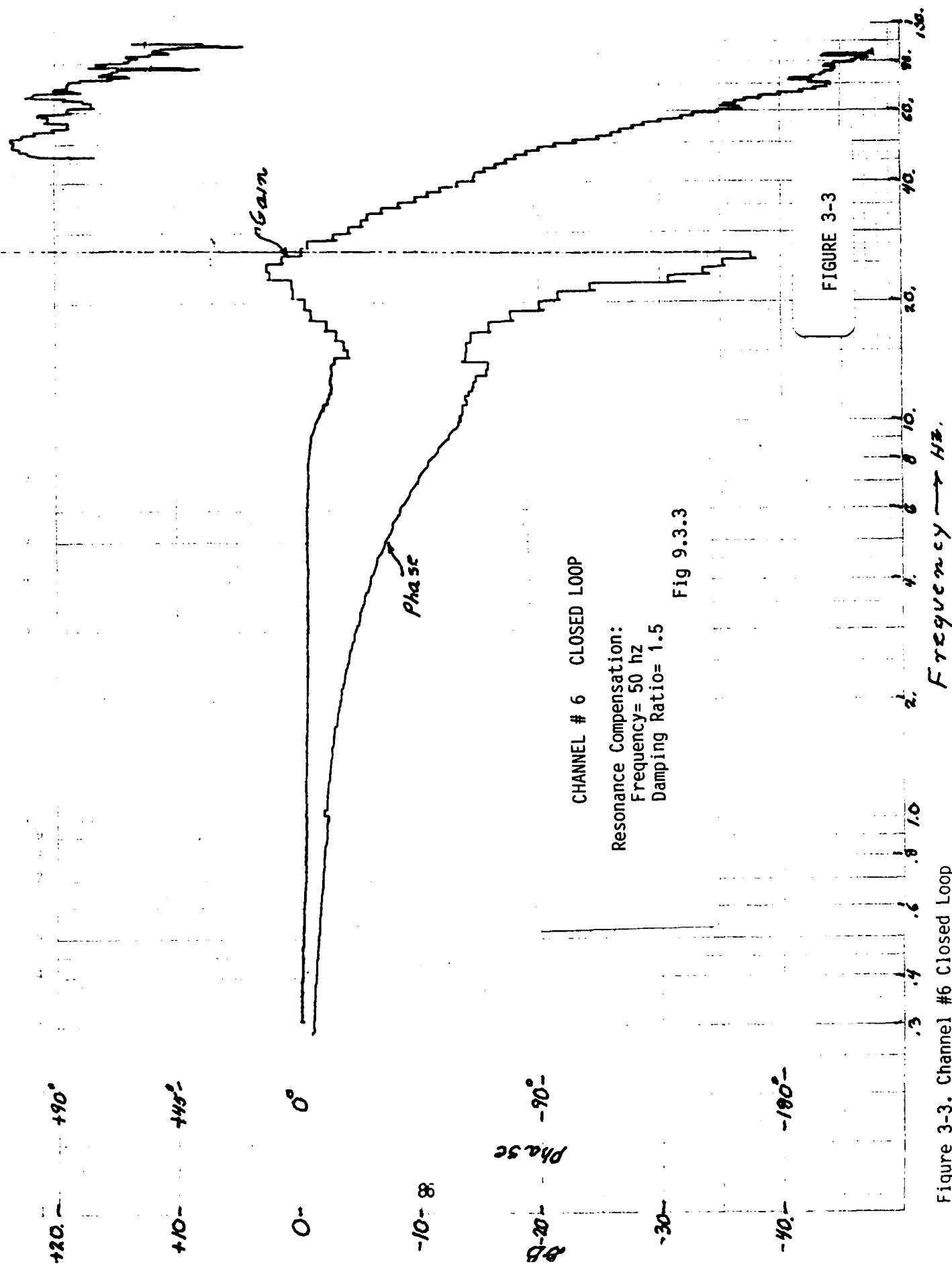


Figure 3-3. Channel #6 Closed Loop

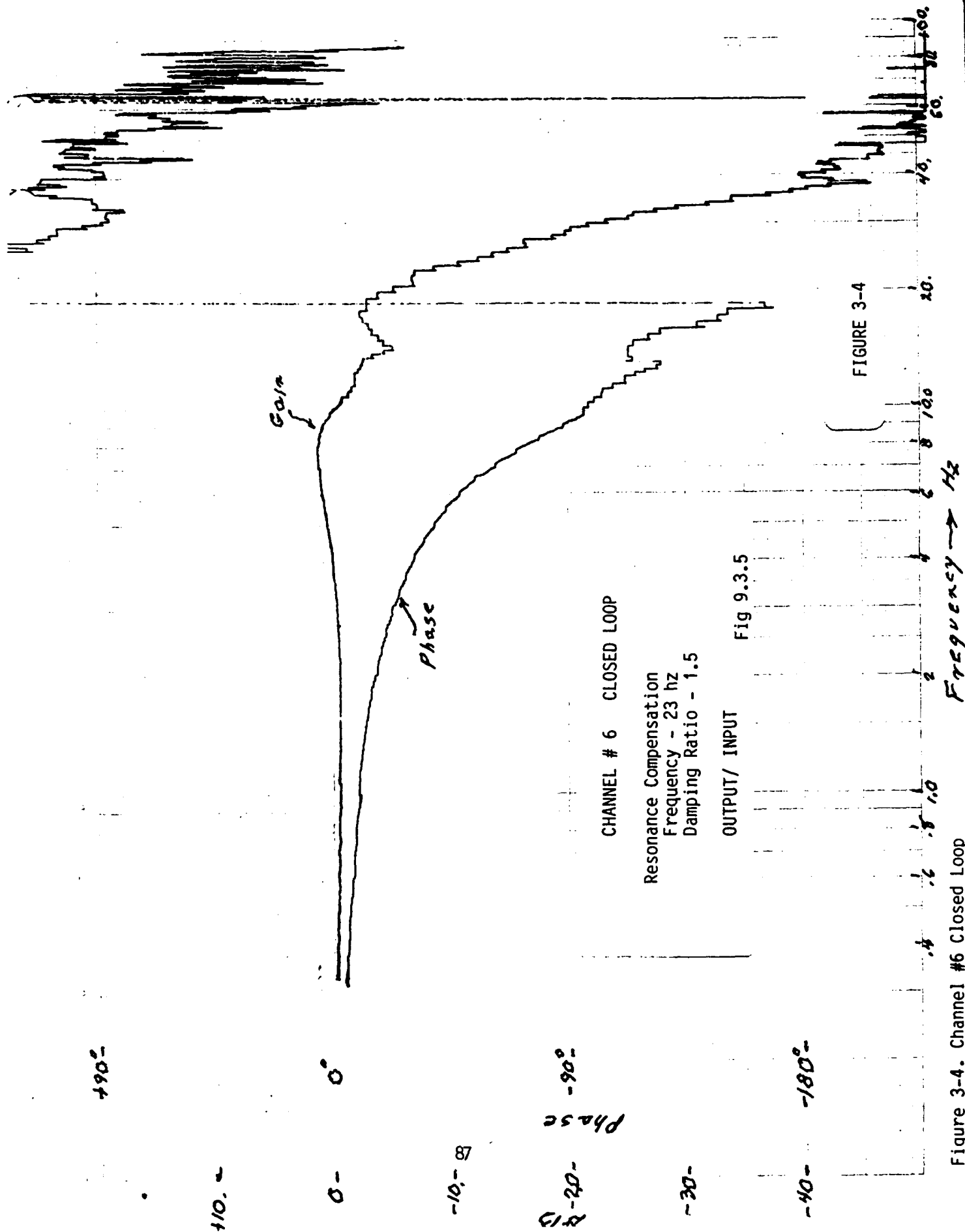


Figure 3-4. Channel #6 Closed Loop

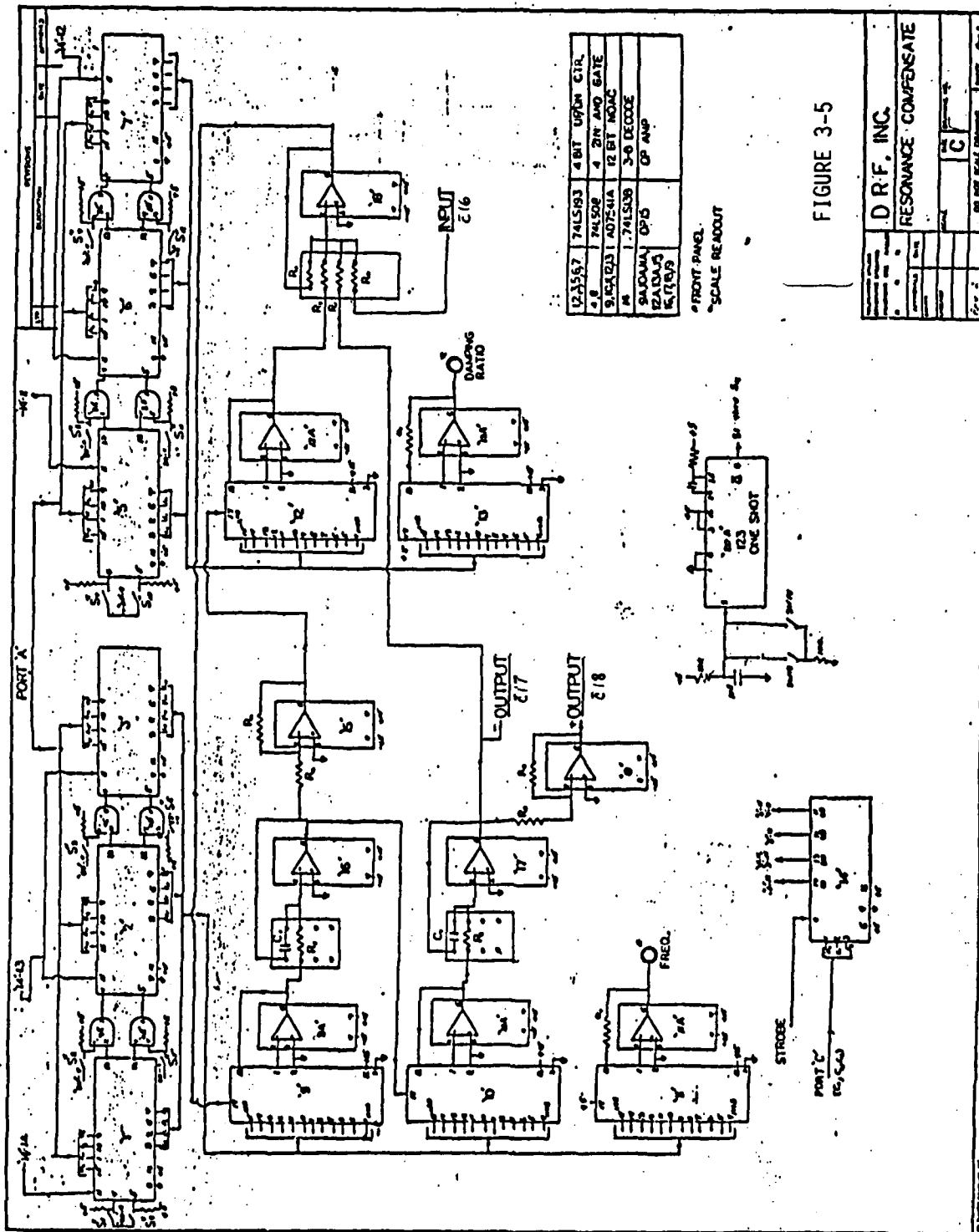
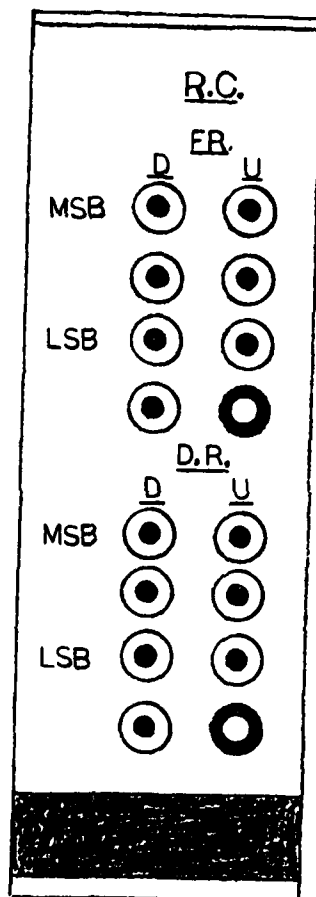


FIGURE 3-5

Figure 3-5. Resonance Compensate



RESONANCE COMPENSATION
FRONT PANEL

FIGURE 3-6

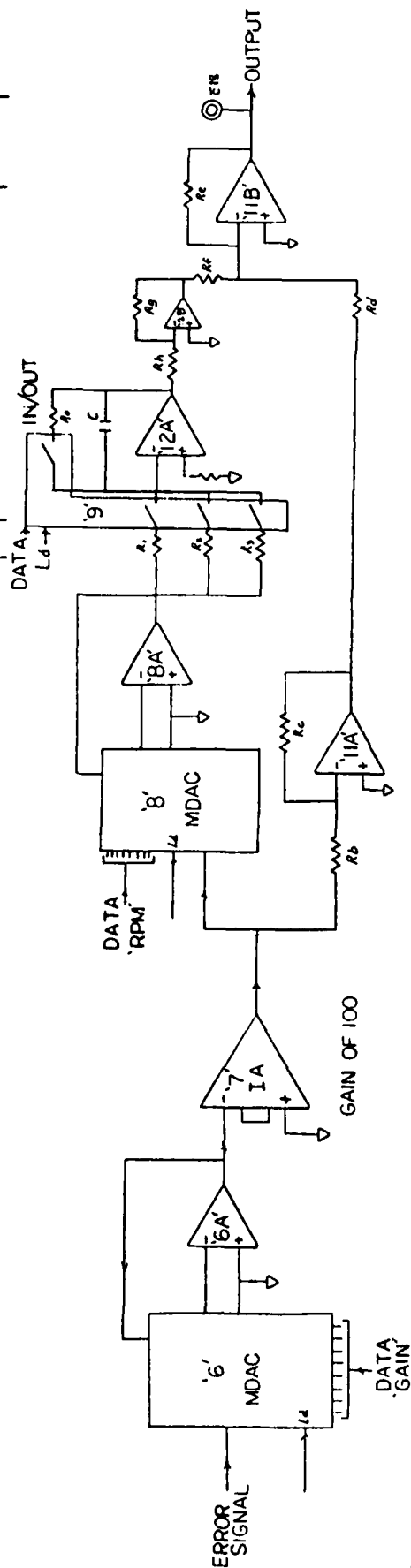
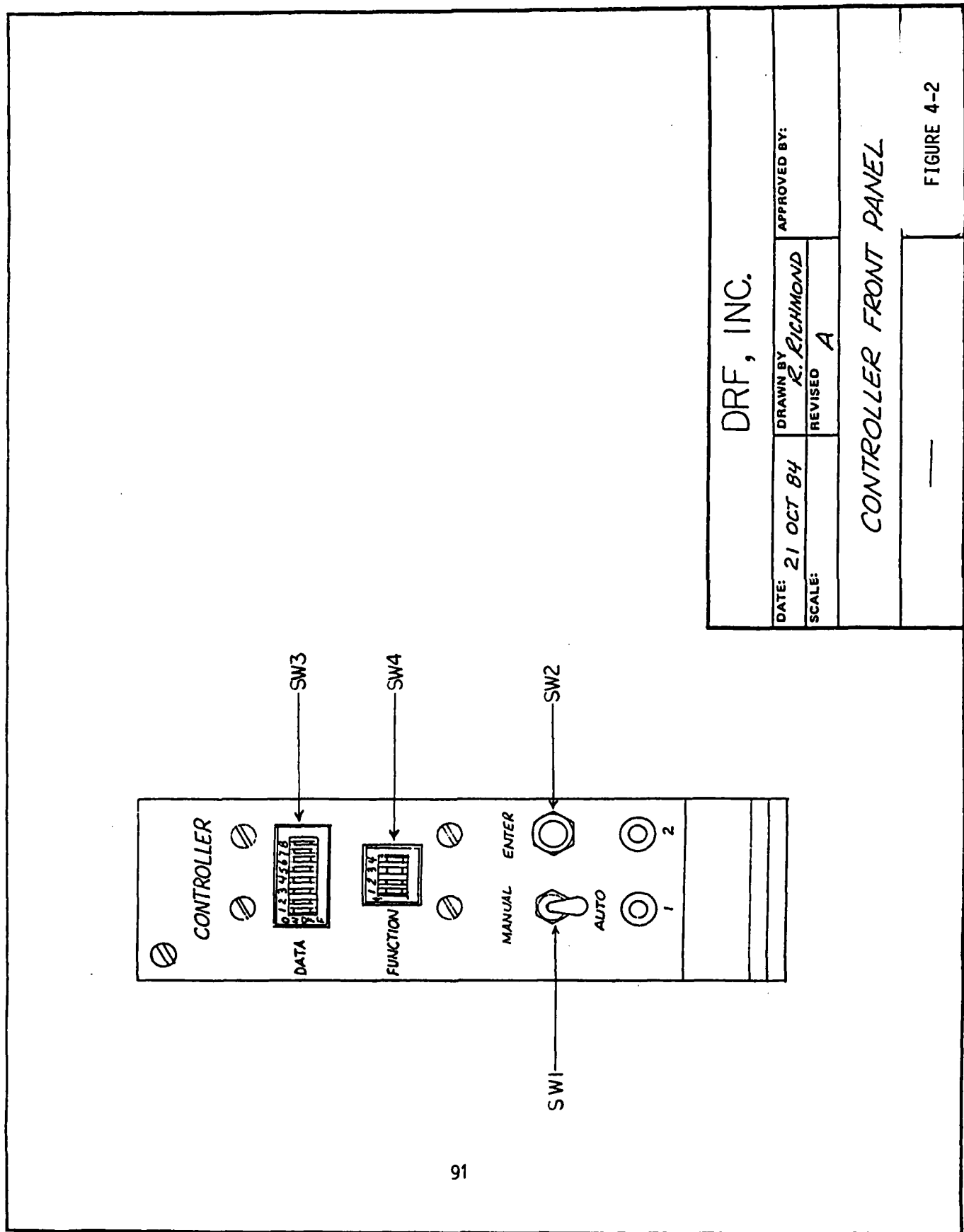


Figure 4-1 Programmable Controller Board



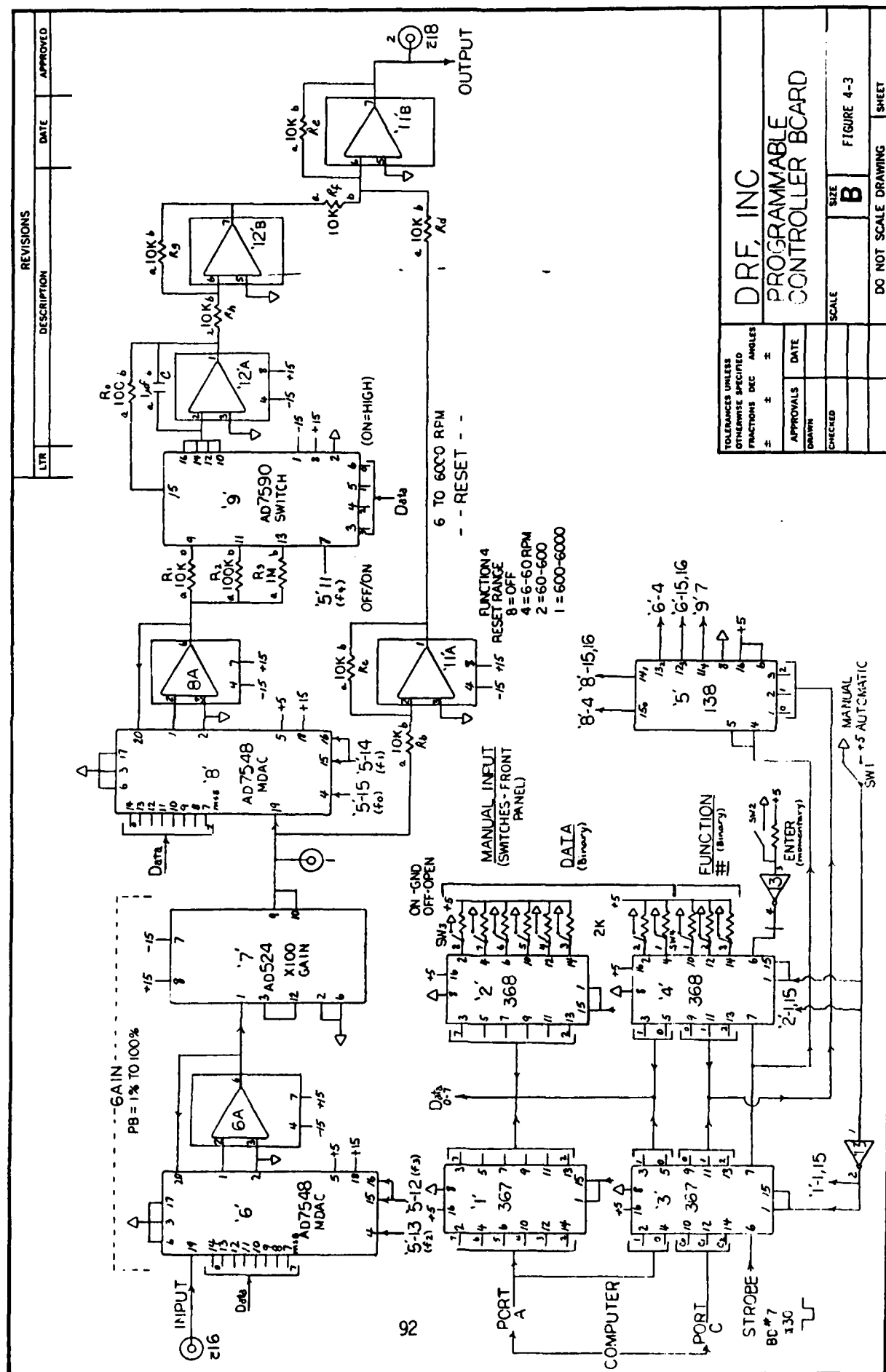


Figure 4-3. Programmable Controller Board

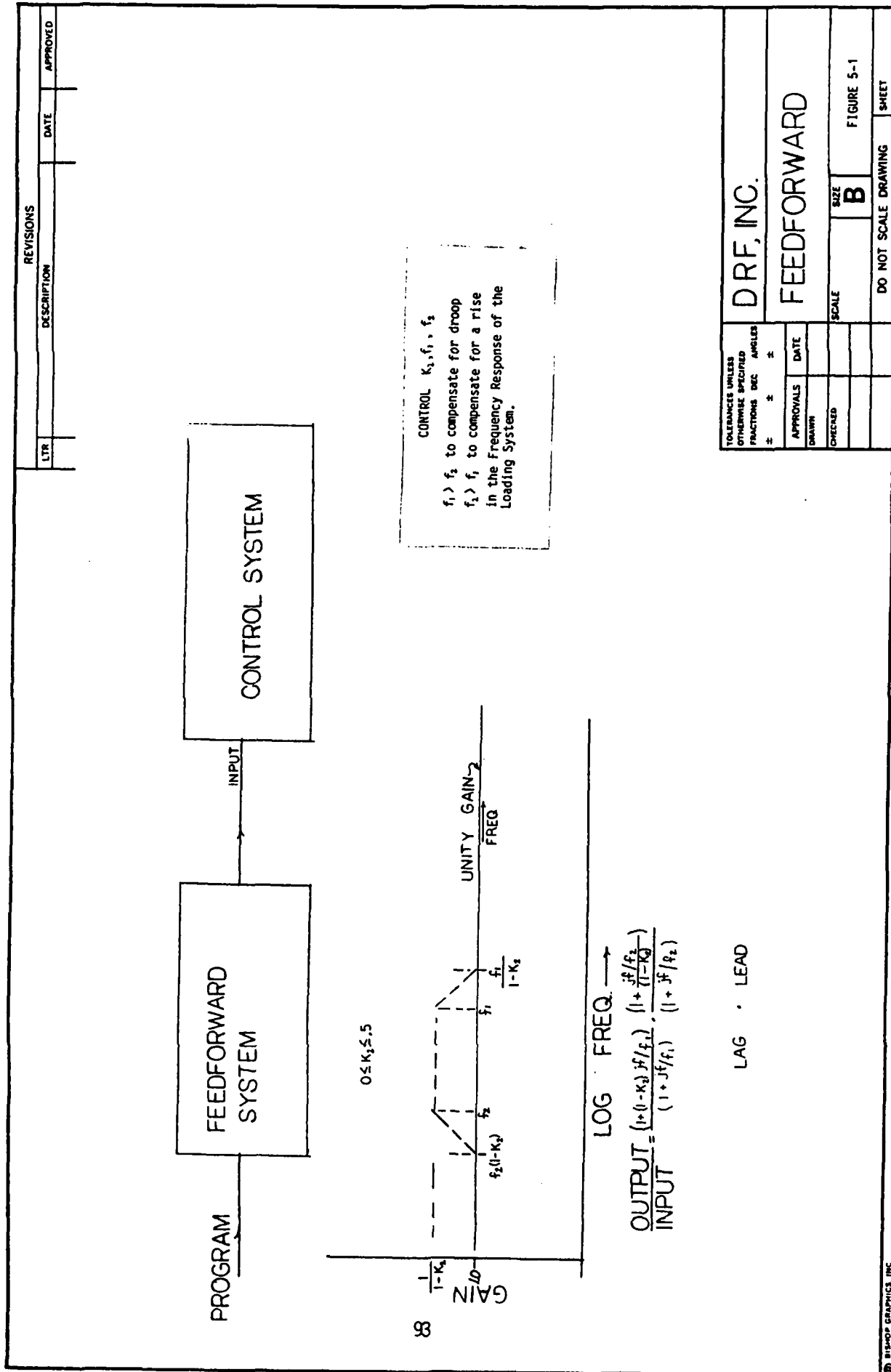


Figure 5-1. Feedforward

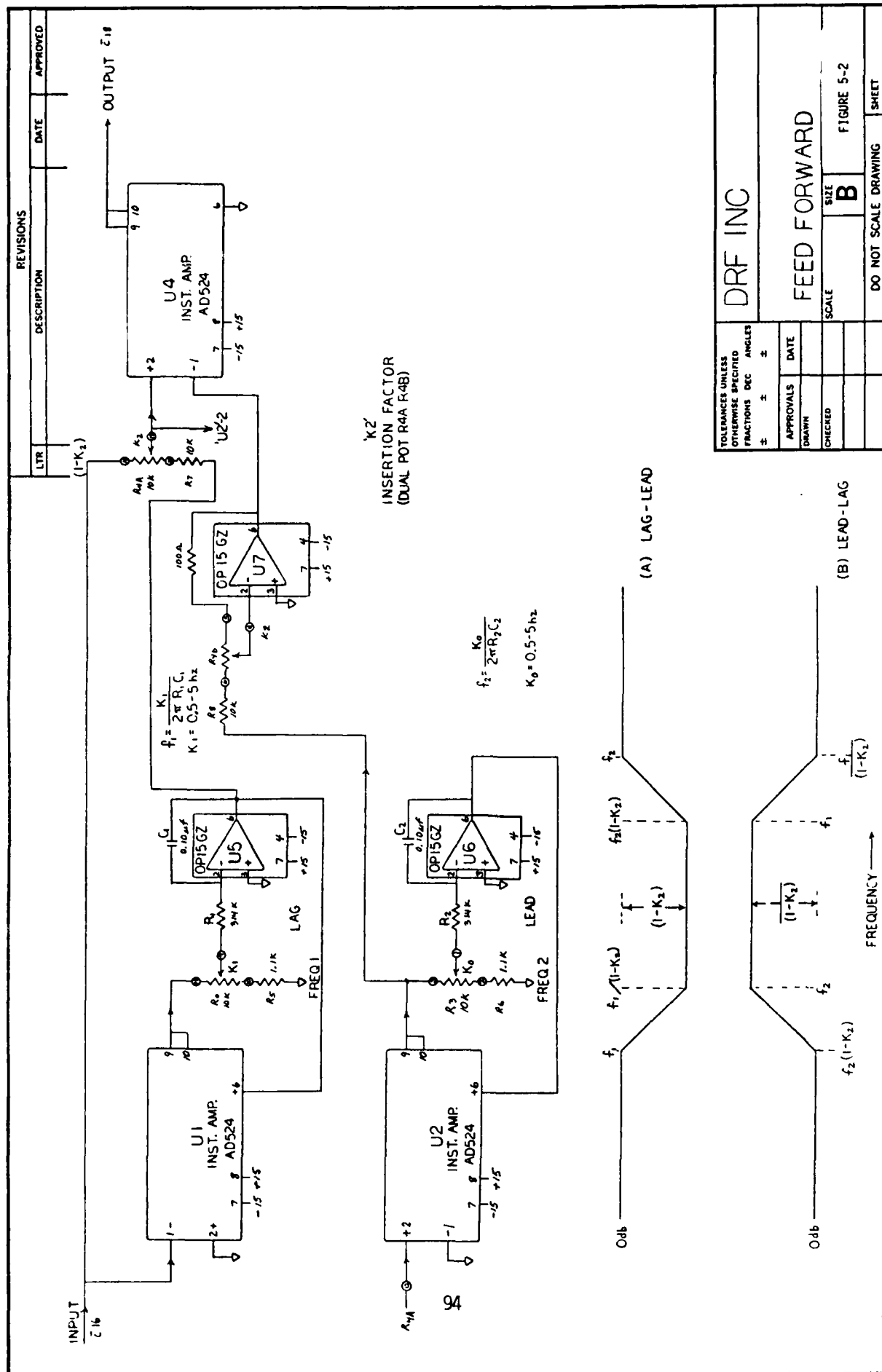
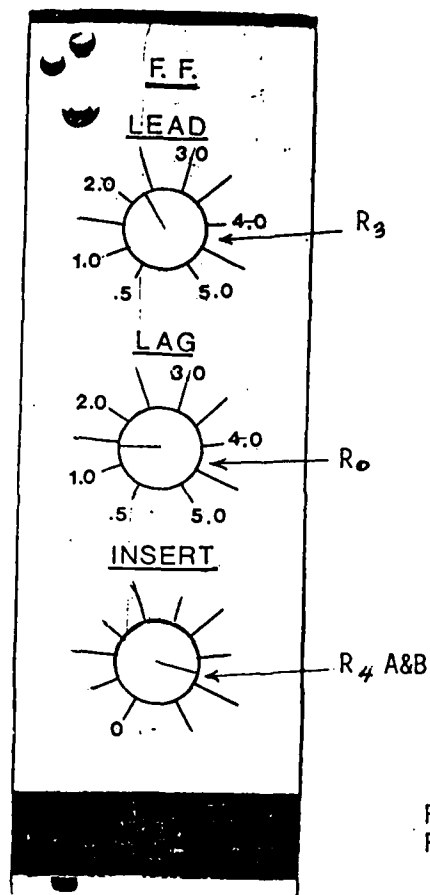


Figure 5-2. Feedforward



FRONT PANEL
FEEDFORWARD NETWORK

FIGURE 5-3

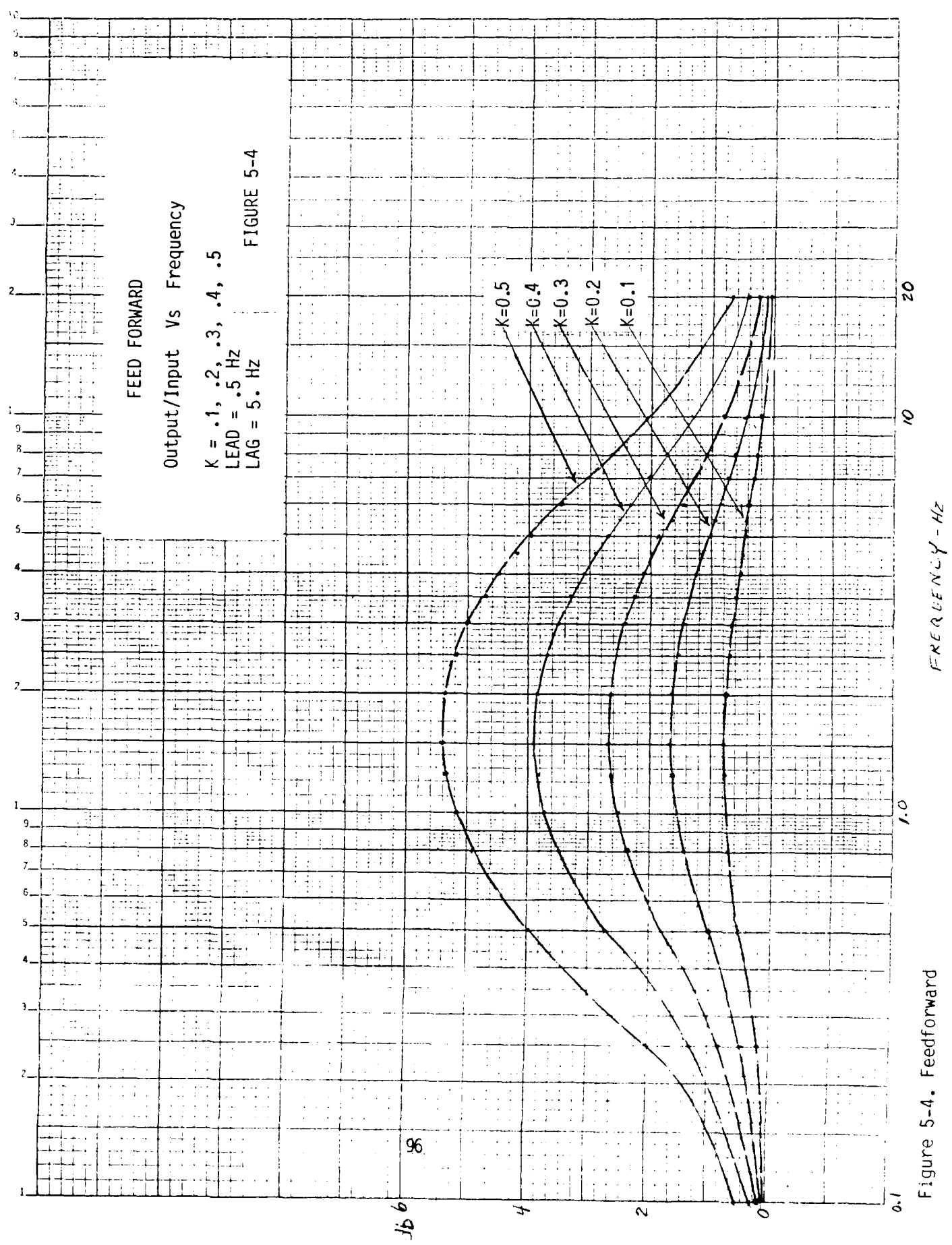


Figure 5-4. Feedforward

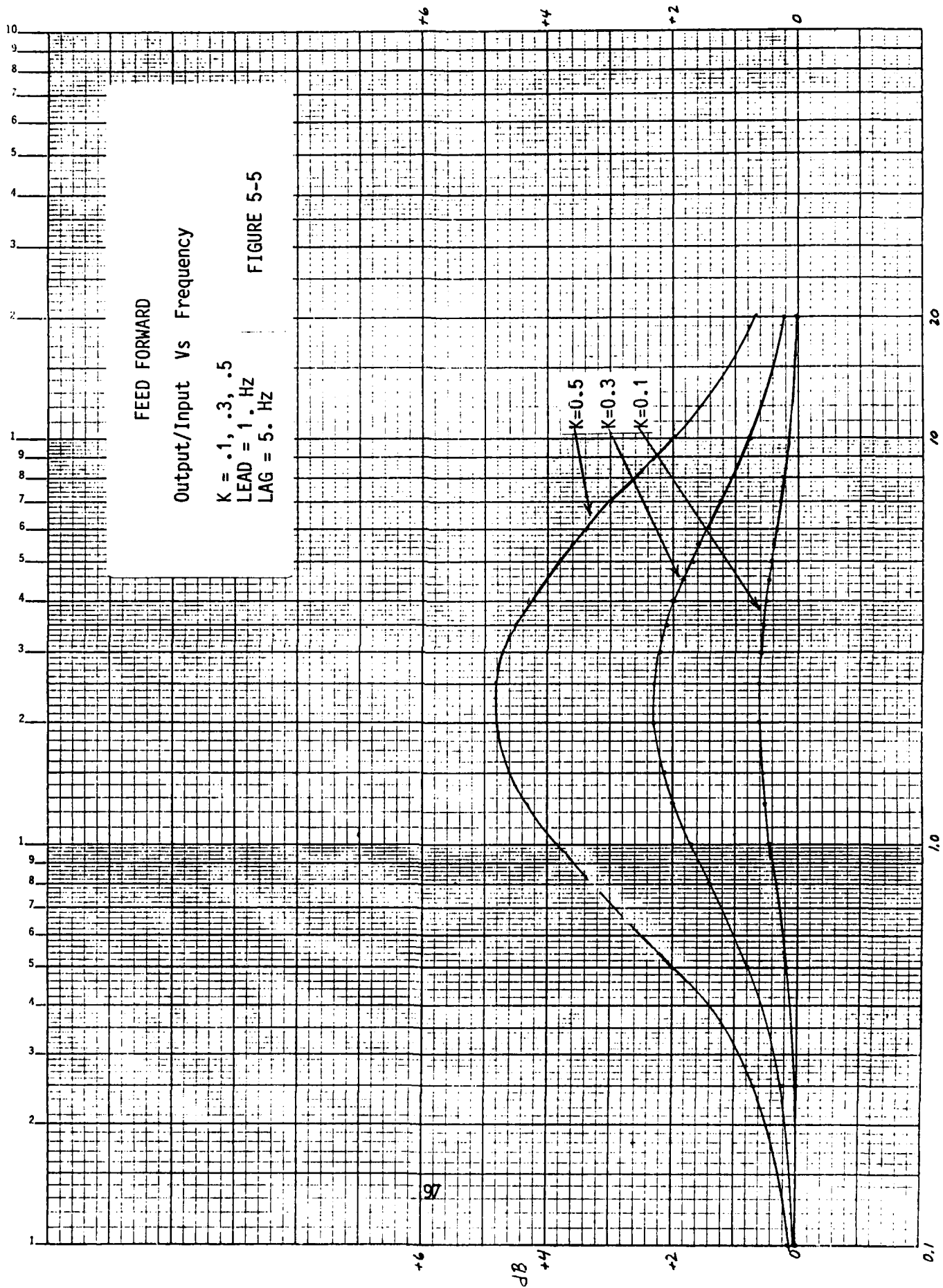


Figure 5-5. Feedforward

FREQUENCY - Hz

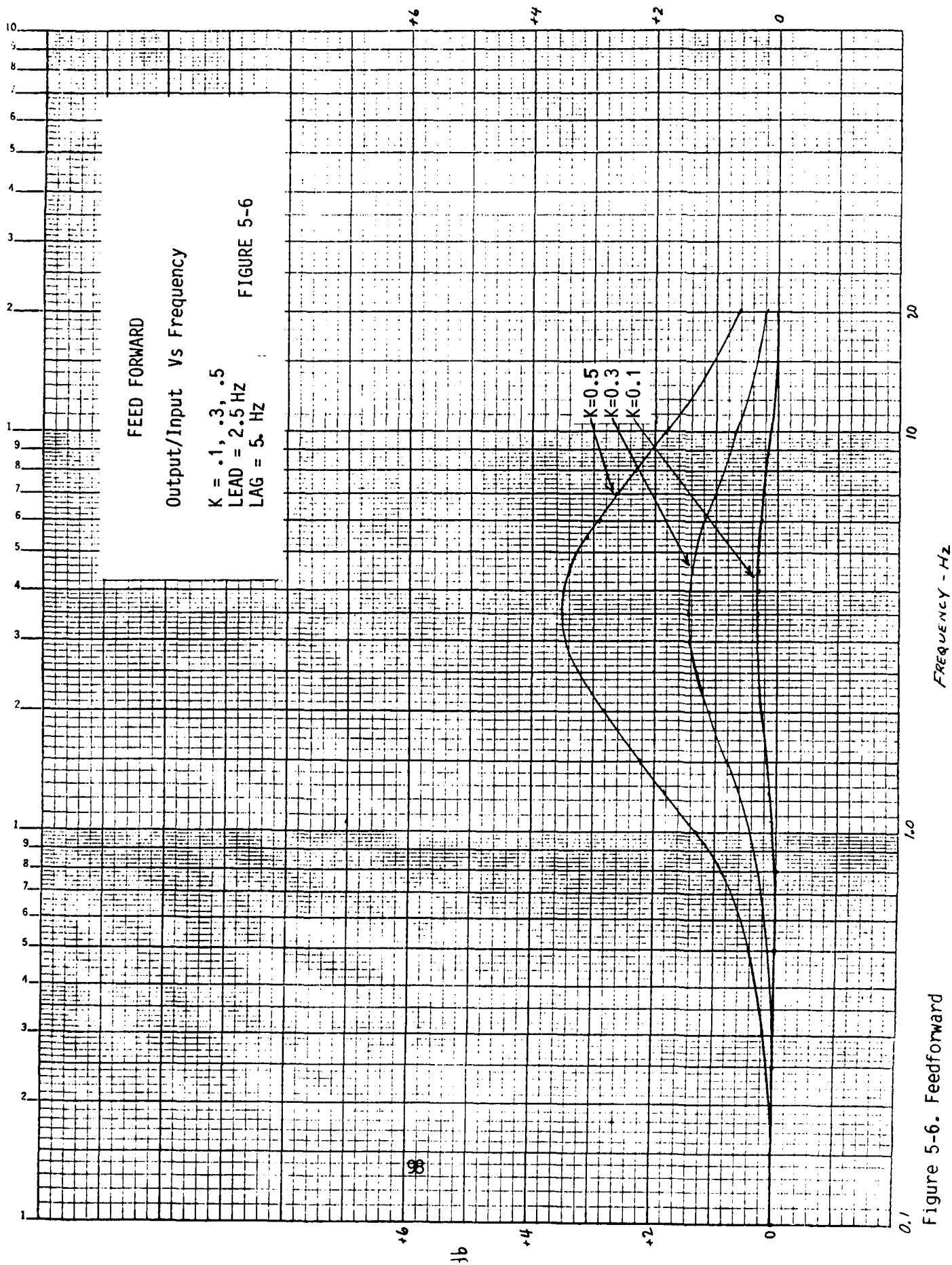


Figure 5-6. Feedforward

Figure 5-7. Feedforward

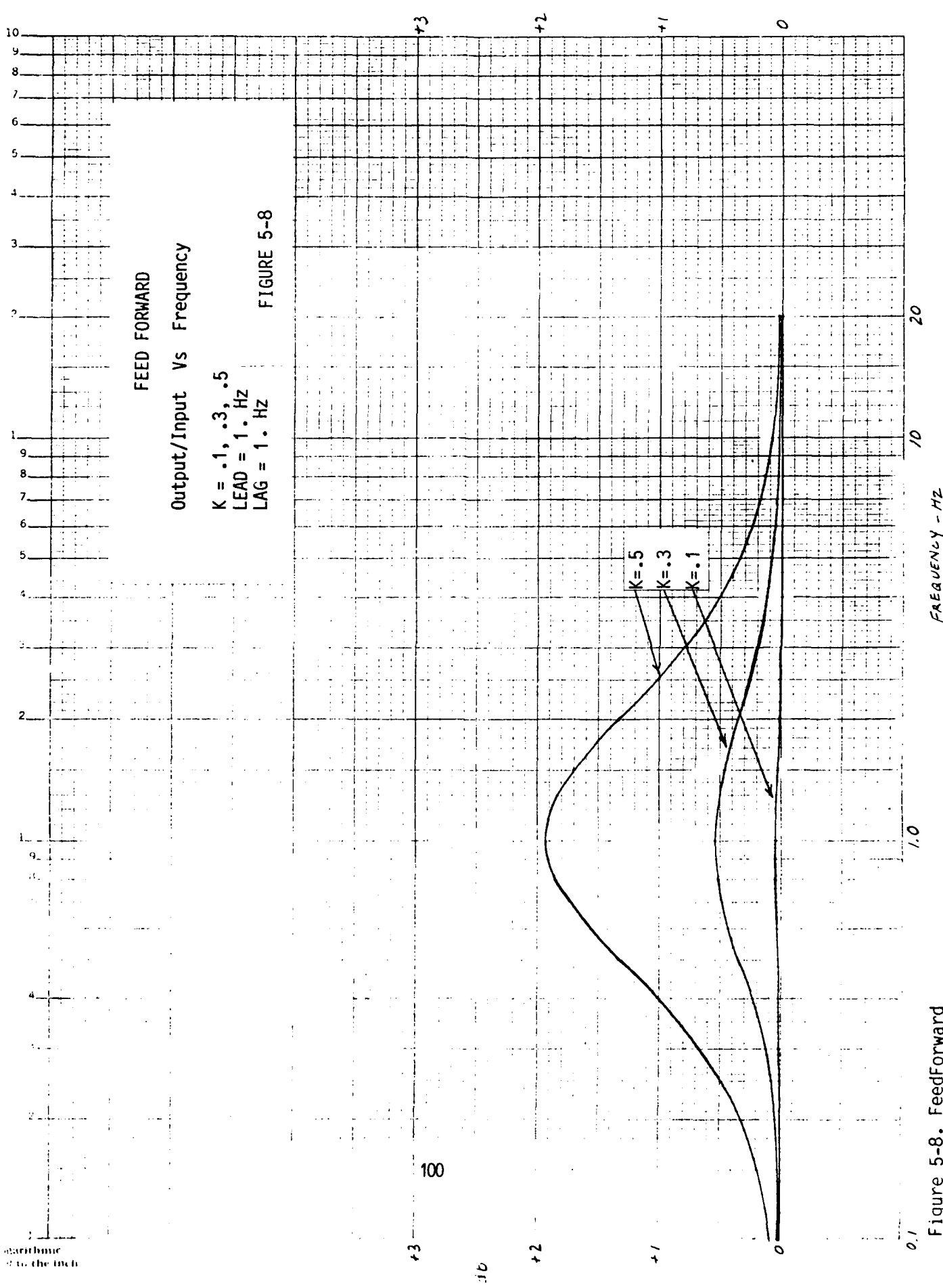


Figure 5-8. FeedForward

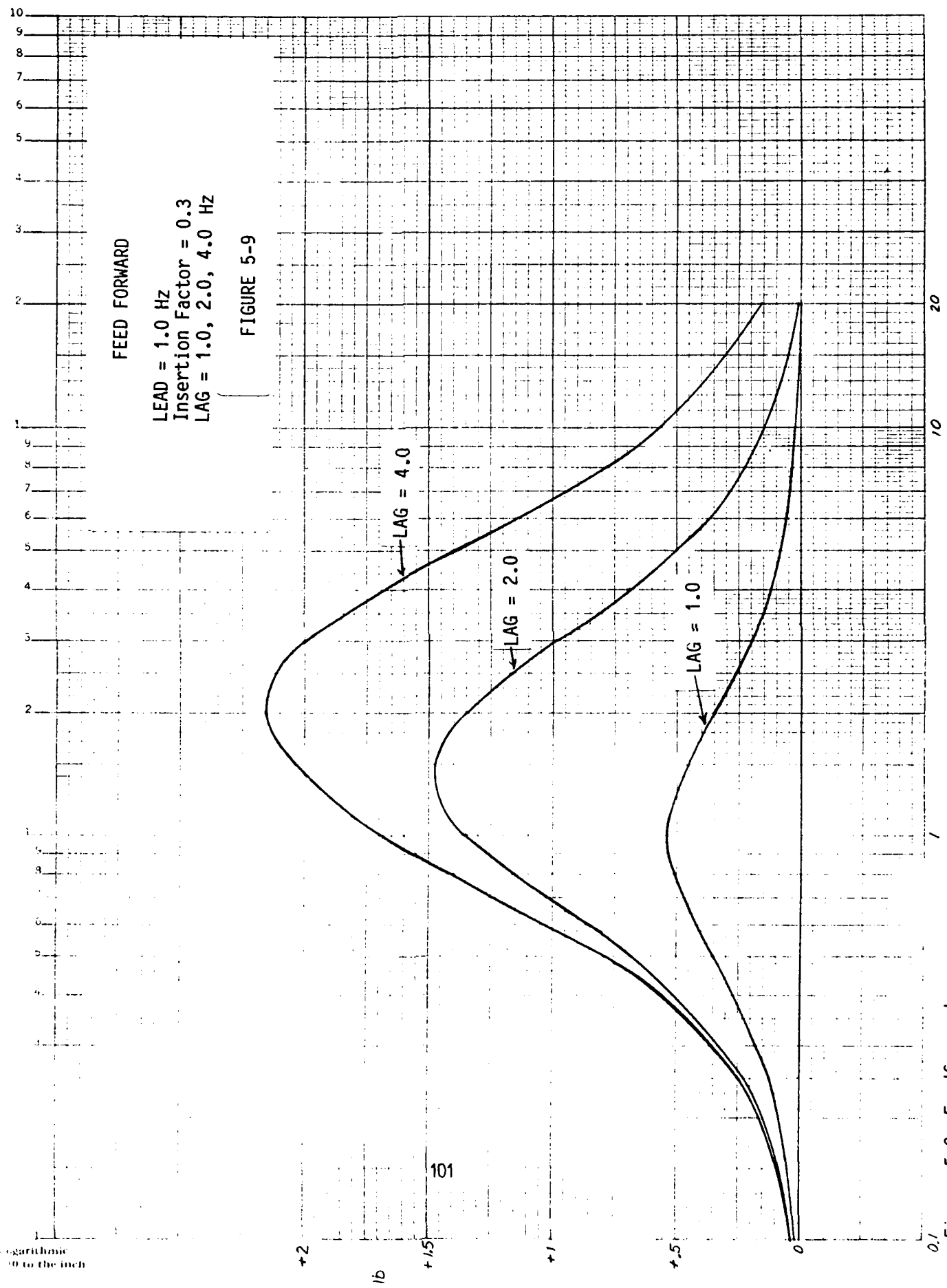


Figure 5-9. Feedforward

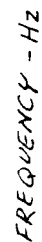


Figure 5-10. Feedforward

FIGURE 6-1

Integral Compensation
Compared to Reset:
Output/Input in DB &
Phase vs Frequency
for Integral Compensation

α = Ratio Second Break
Frequency
to
First Break
Frequency

Output/Input

$$(ju) = \alpha \frac{ju + 1}{j\alpha u + 1}$$

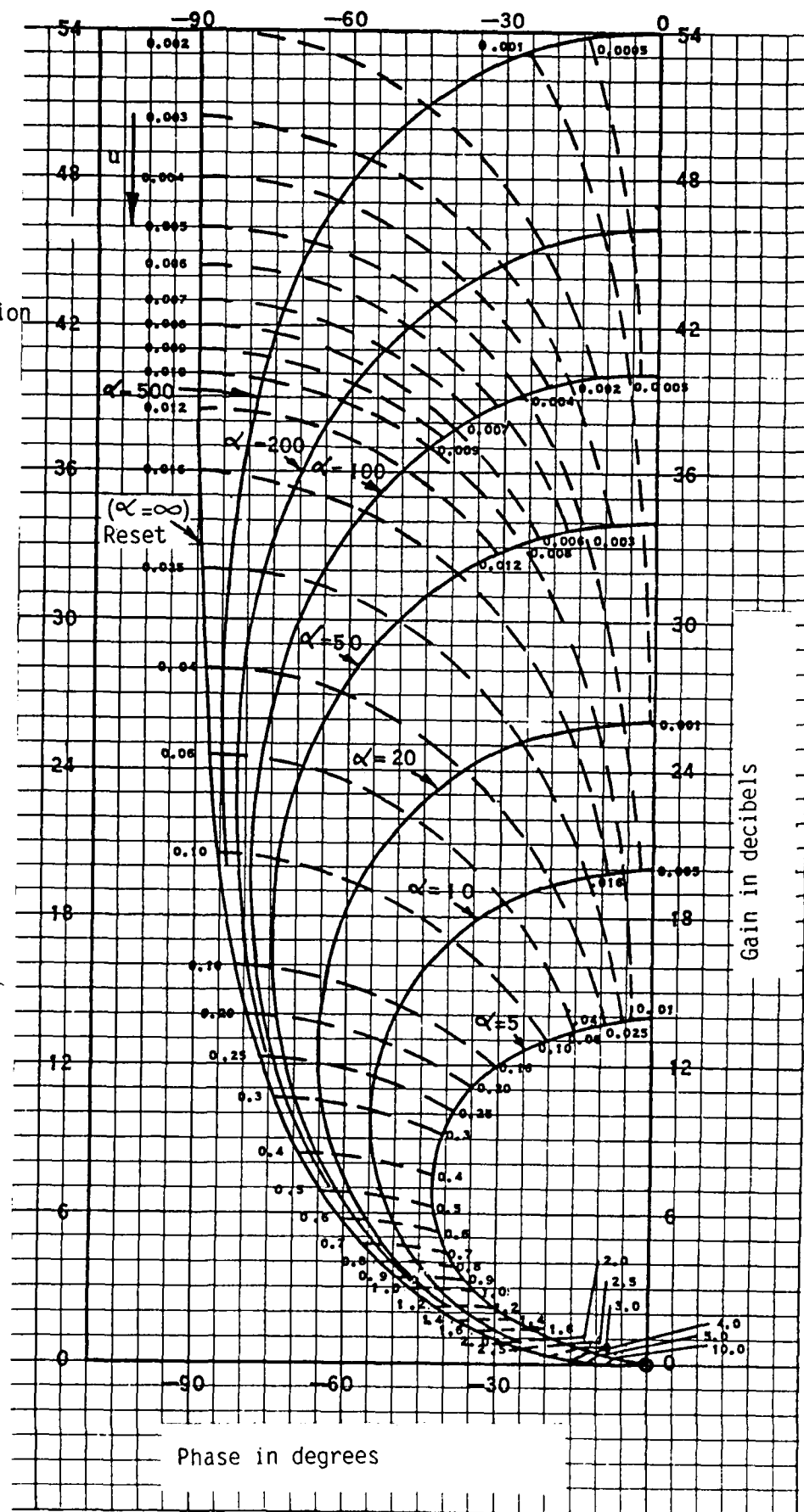


Figure 6-1. Integral Compensation Compared to Reset

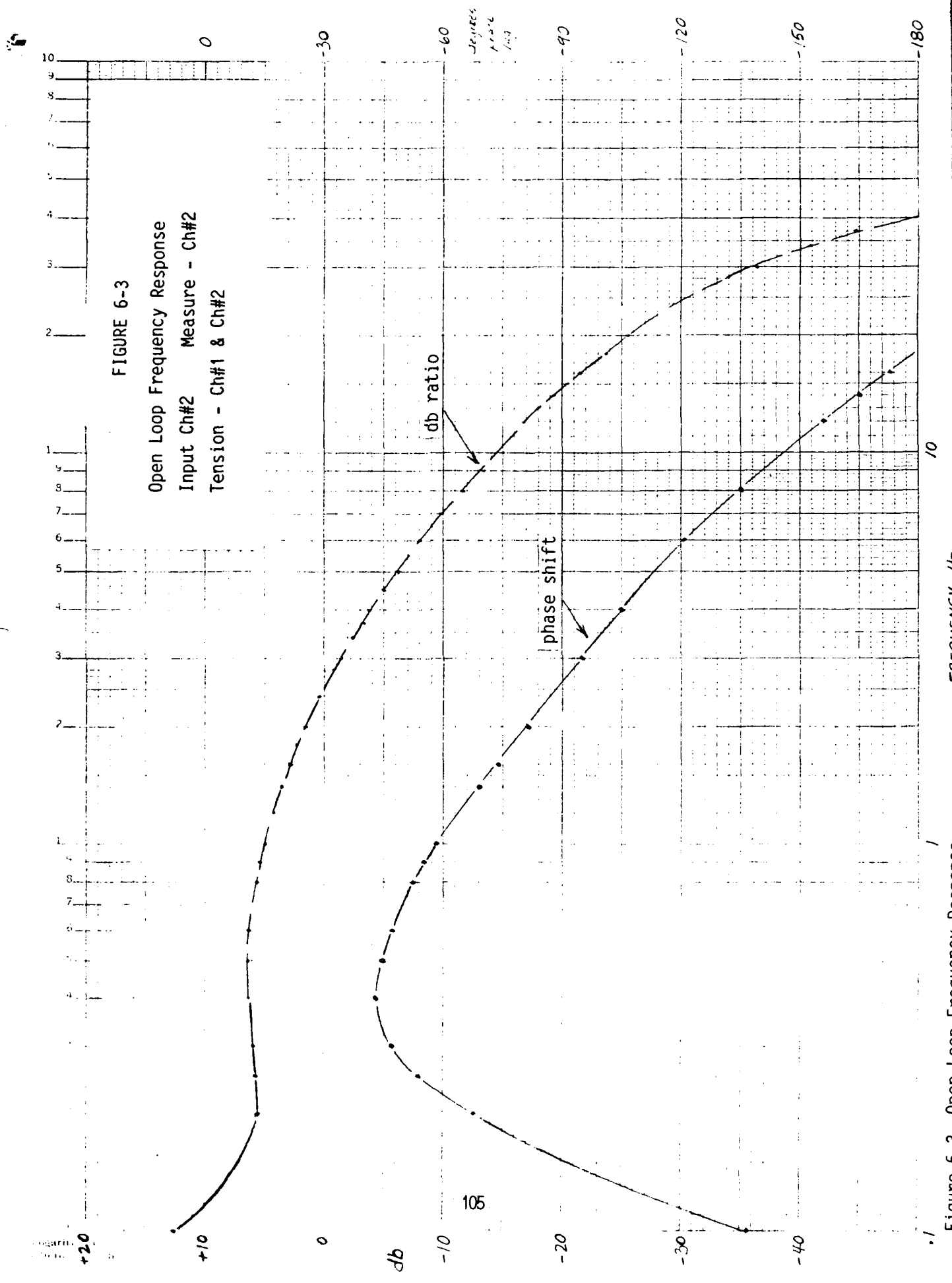


FIGURE 6-3

Open Loop Frequency Response
 Input Ch#2 Measure - Ch#2
 Tension - Ch#1 & Ch#2

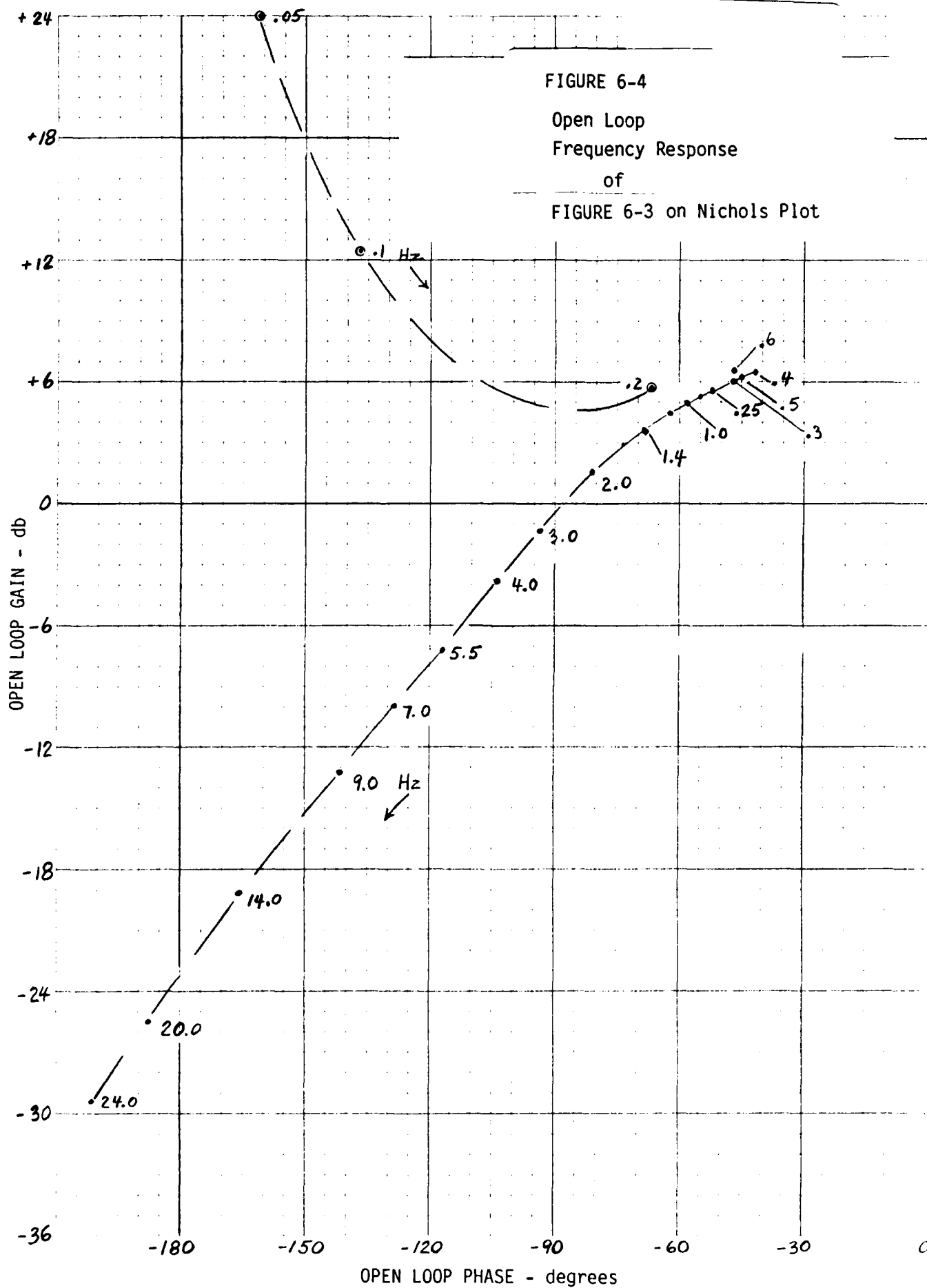
Figure 6-3. Open Loop Frequency Response

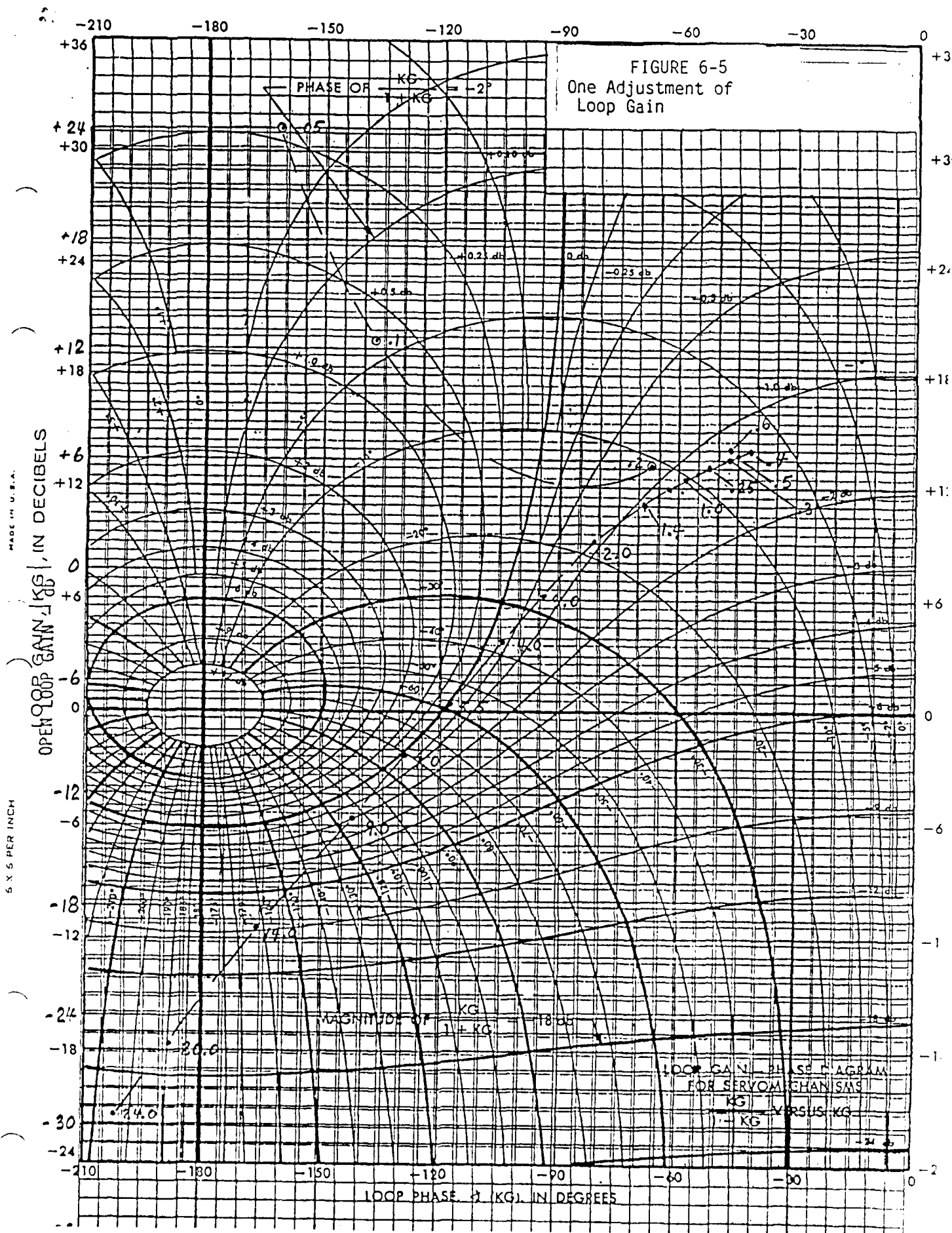
FIGURE 6-4

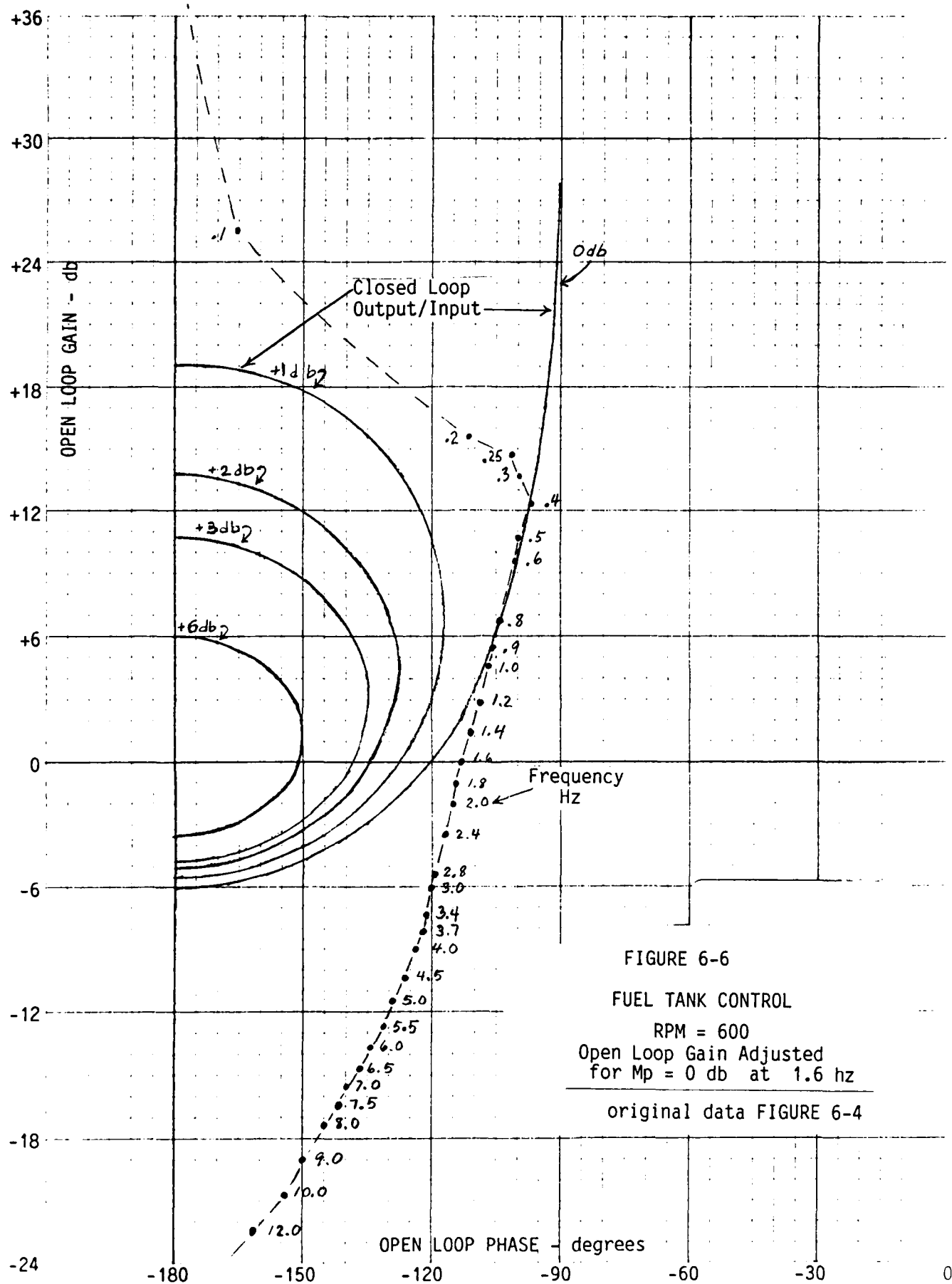
Open Loop
Frequency Response

of

FIGURE 6-3 on Nichols Plot







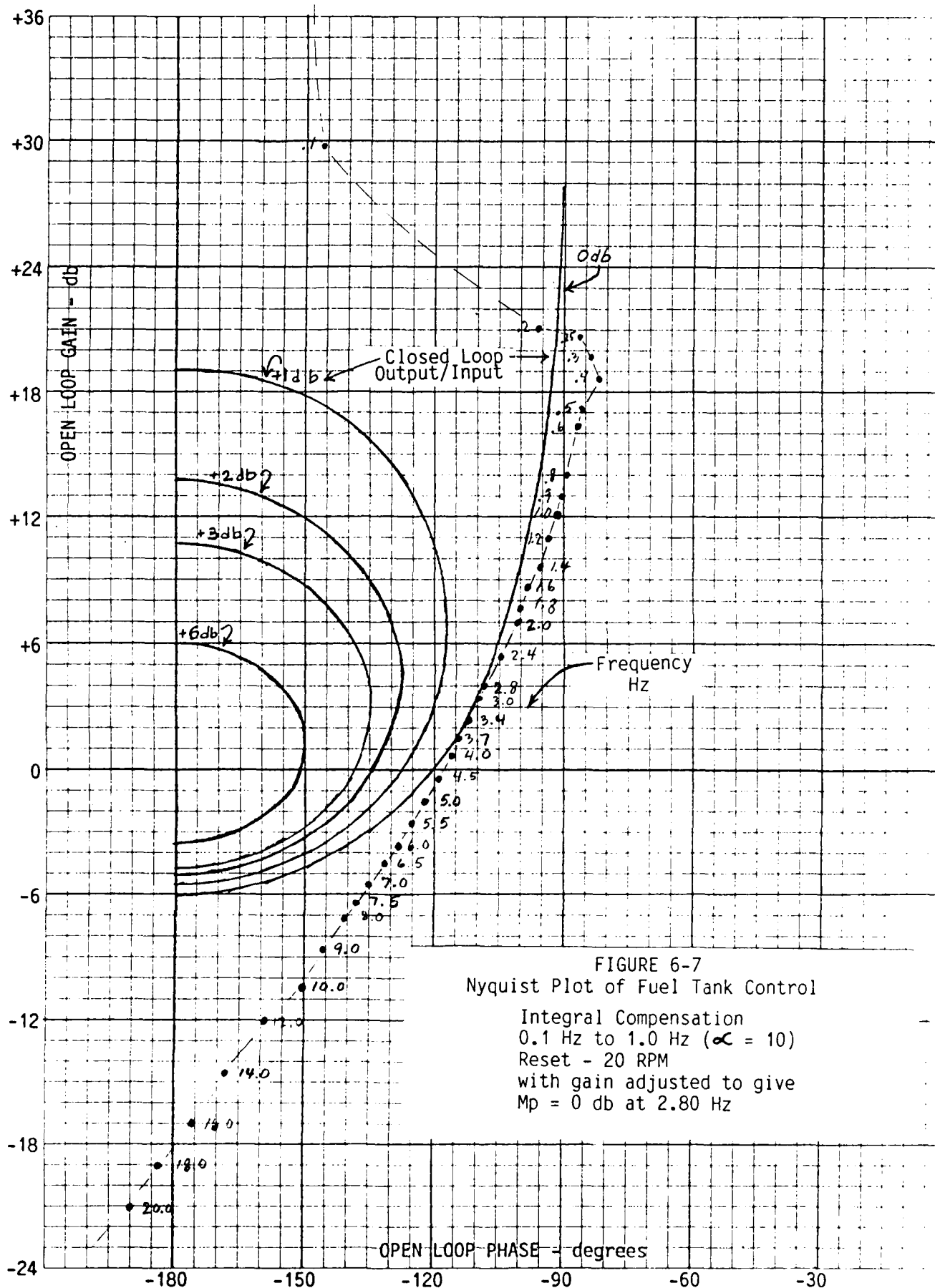


FIGURE 6-7
Nyquist Plot of Fuel Tank Control

Integral Compensation
0.1 Hz to 1.0 Hz ($\alpha = 10$)
Reset - 20 RPM
with gain adjusted to give
 $M_p = 0$ db at 2.80 Hz

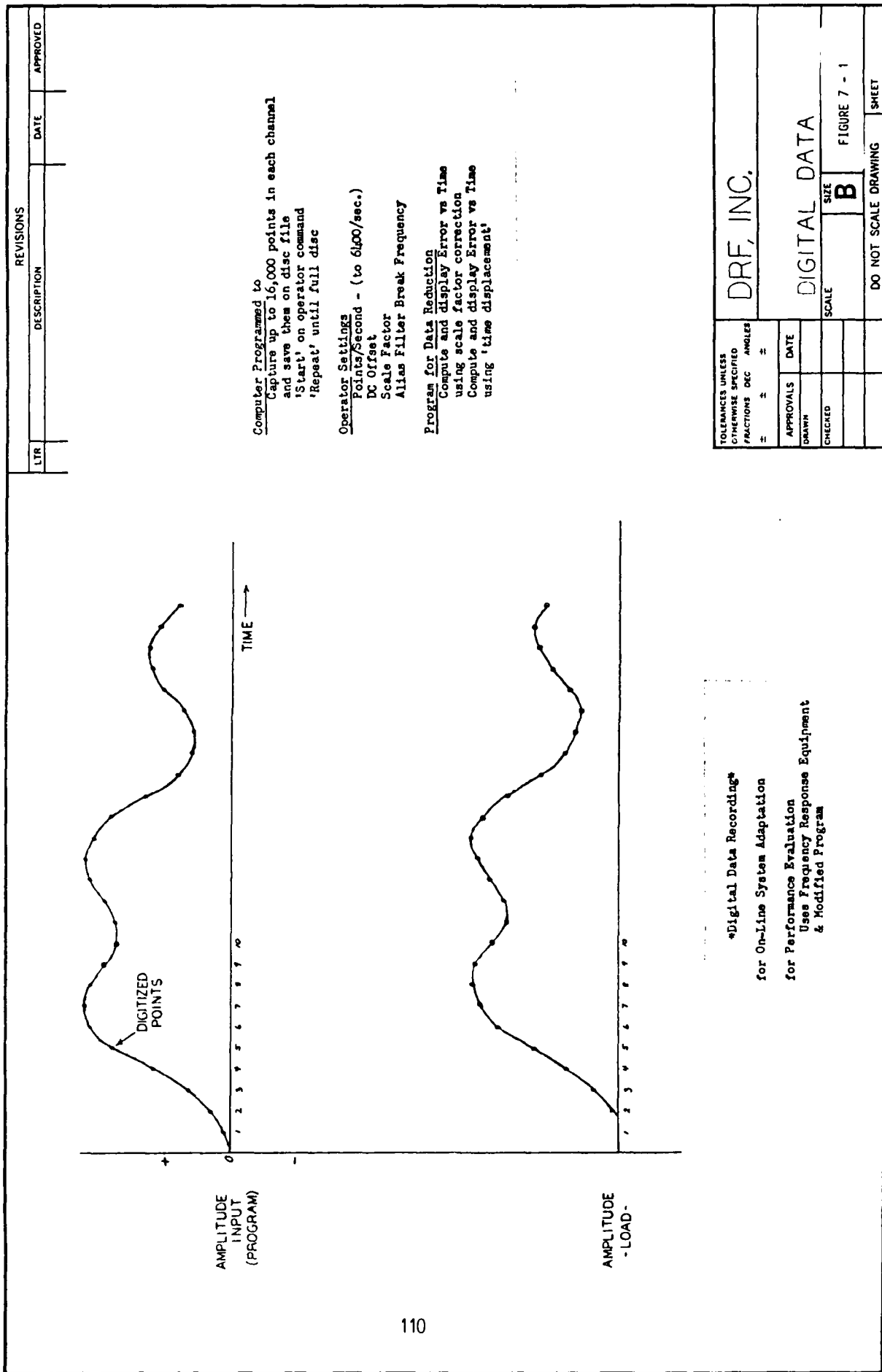


Figure 7-1. Digital Data

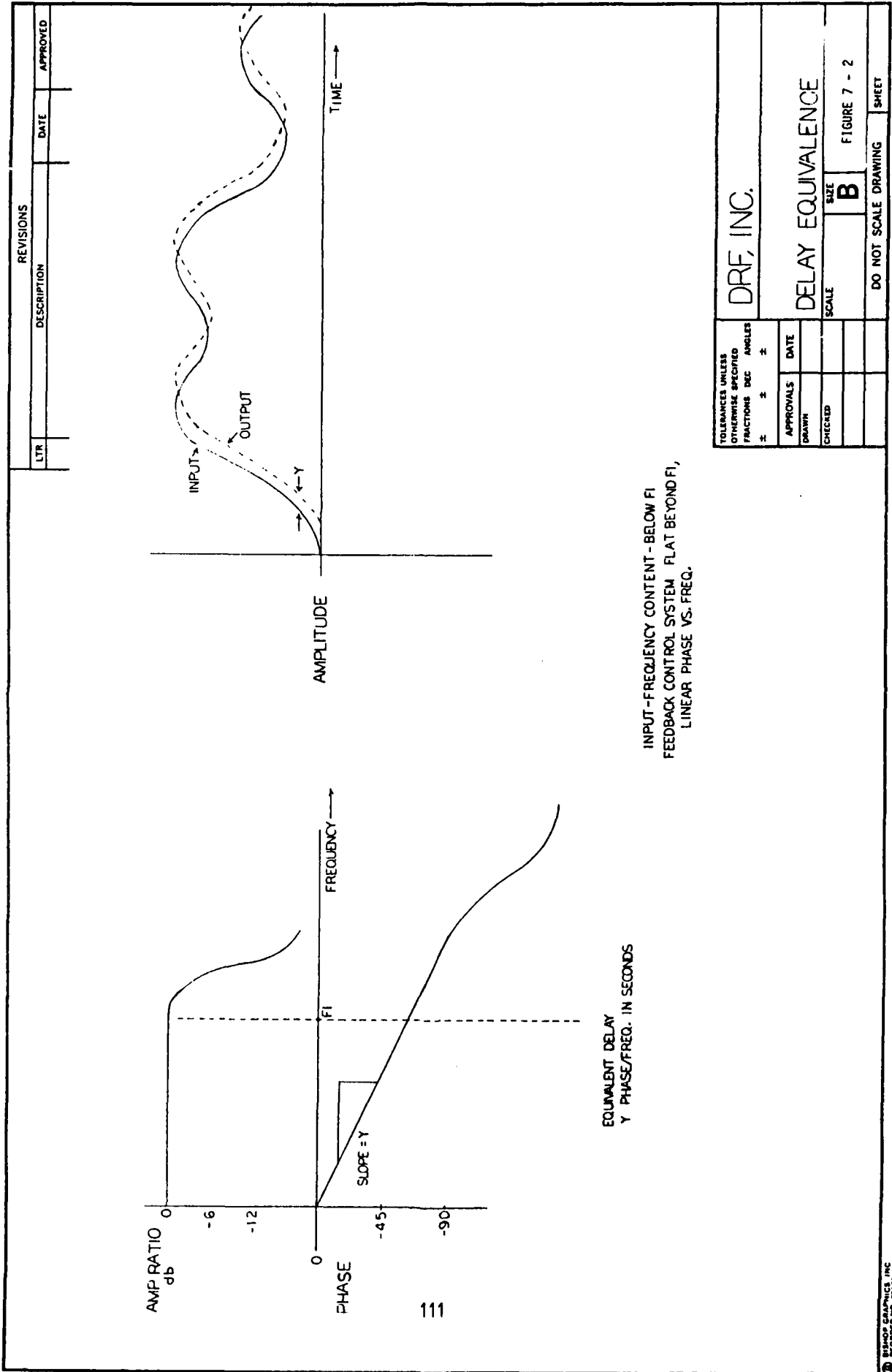
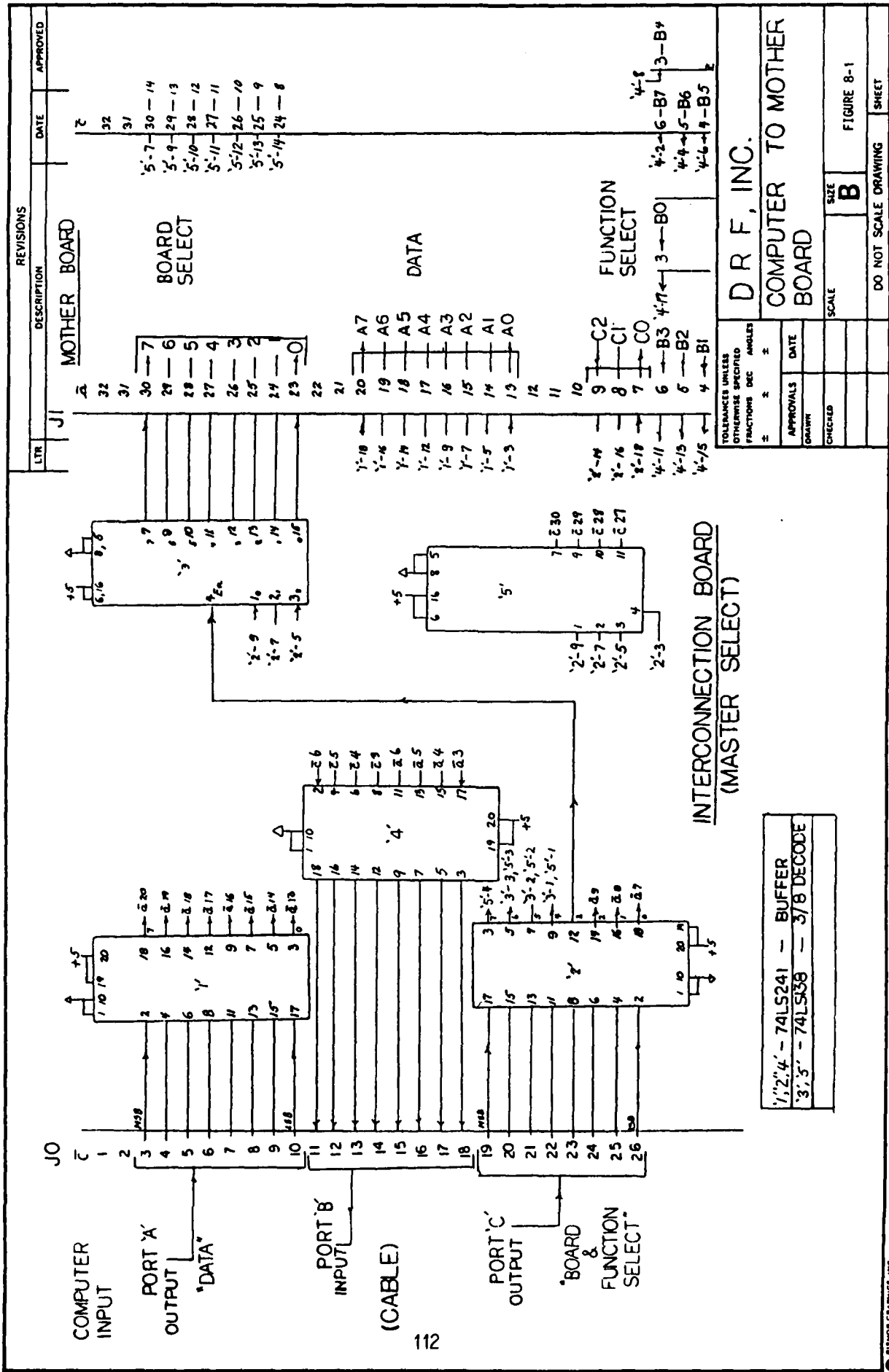
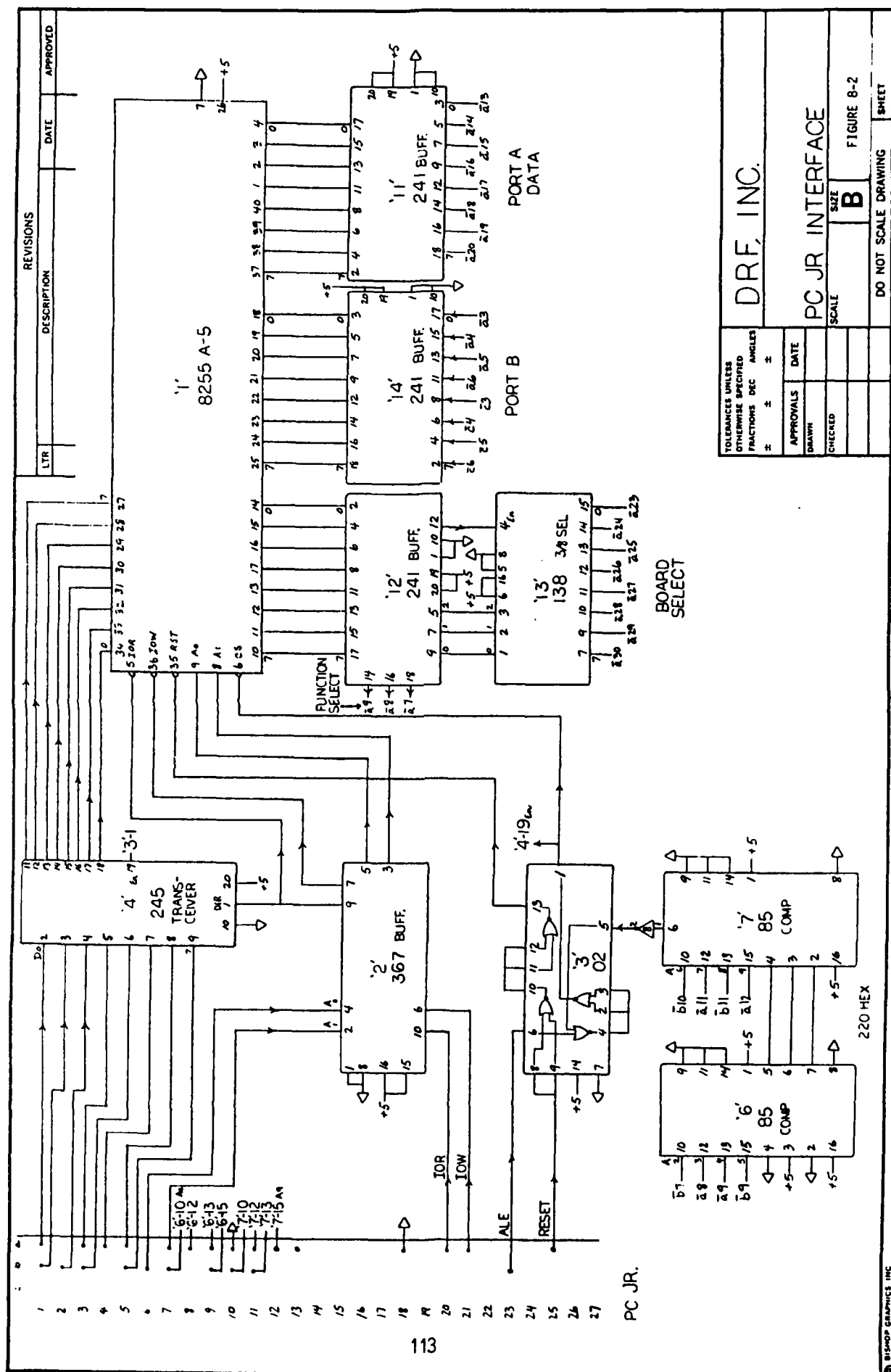


Figure 7-2 Delay Equivalence





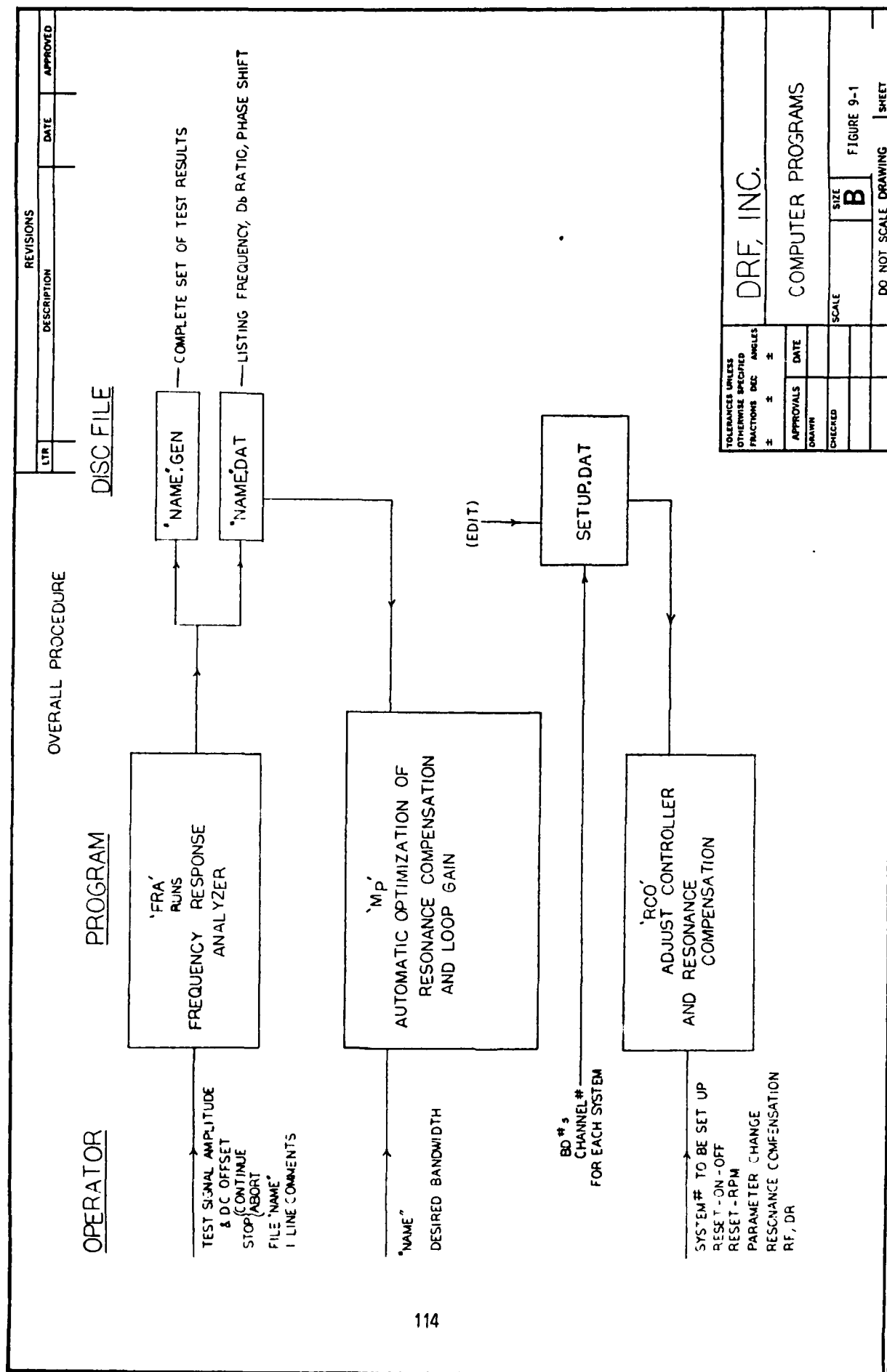
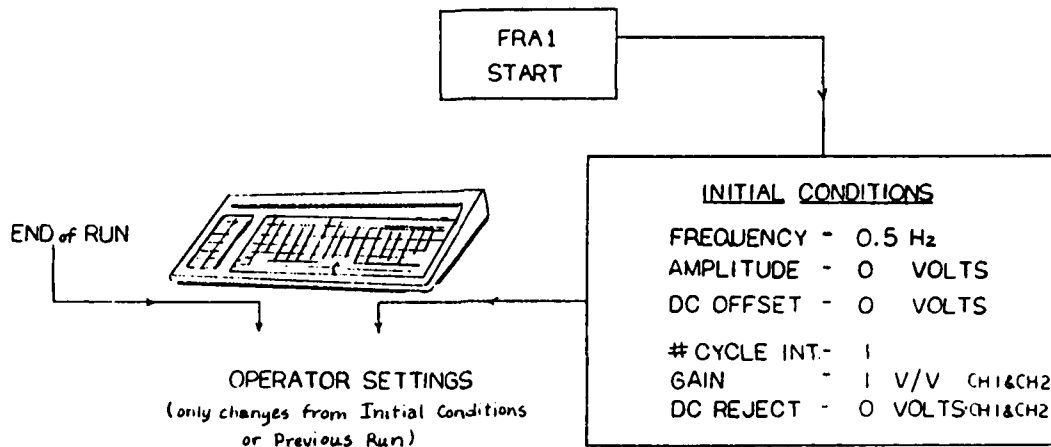


Figure 9-1 Computer Programs



F **ENTER** Enter - 'F'requency
 Prompt₁ - Frequency in Hz from .01 thru 100.0
 Enter - 50
 Prompt₂ - "Frequency = 50.000 Hz"
 Error in Entry
 Prompt₃ - "Incorrect entry - try again"

A **ENTER** Enter - 'A'mplitude
 Prompt₁ - "Amplitude = X.XXXX to 9.9999 volts peak"
 Enter - 0.43
 Prompt₂ - "Amplitude command is .4300 volts peak"
 Error - "Incorrect entry - try again"

D **ENTER** Enter - 'D'C Offset
 Prompt₁ - "DC Offset X.XXXX +- 9.999 volts"
 Enter - -3.62
 Prompt₂ - "DC Offset command is -3.6200 volts"
 Error - "Incorrect entry - try again"

I **ENTER** Enter - # cycles 'I'ntegrated
 Prompt₁ - "# cycles to be integrated over - 1,2,4,8"
 Enter - 2
 Prompt₂ - "Number of cycles = 2"
 Error- "Error - try again"
 (# cycles set = 1)

DO NOT SCALE DRAWING		SCALE	SIZE	FRA SET UP	DRG. INC.
			B		
		FIGURE 10-1			
		SHEET			

VG 5.1-2

REVISIONS		
ITER	DESCRIPTION	DATE

Figure 10-1 FRA Set Up

CL amp - Closed Loop (Data
 Oamp - Closed Loop adjusted for Mp=0 db above 1.0 hz
 Amplitude Ratio db vs Frequency

```

19
20 file name ?
21 p1-trial.dat
22 Peak at 7.00 Hz ; delta_gain = 14.71 db for Mp= 0 db
23 Max LF DEV = -2.41 db: -1 db BW= 8.00 Hz : -20db at 20.00 Hz
24 closed loop adjusted for Mp=0 db
25 data file being analyzed - p1-trial.dat;
26
27 FREQ OL amp: CL amp Oamp : FREQ OL amp: CL amp Oamp
28 0.10 8.24 2.88 0.51 7.00 -16.15 -15.39 0.00
29 0.15 2.09 1.32 0.66 7.50 -17.14 -16.36 -0.02
30 0.20 -1.85 -3.12 0.16 8.00 -18.11 -17.35 -0.36
31 0.30 -4.95 -6.95 -1.00 9.00 -19.97 -19.28 -1.69
32 0.40 -6.32 -8.66 -1.83 10.00 -21.69 -21.08 -3.50
33 0.60 -6.46 -9.29 -2.34 12.00 -23.82 -23.30 -5.95
34 0.80 -6.44 -9.32 -2.37 14.00 -26.70 -26.30 -9.60
35 1.00 -6.56 -9.40 -2.41 16.00 -29.03 -28.72 -12.49
36 1.20 -6.63 -9.43 -2.40 18.00 -31.28 -31.04 -15.18
37 1.40 -6.84 -9.53 -2.41 20.00 -33.77 -33.59 -18.05
38 1.60 -6.98 -9.56 -2.38 24.00 -38.50 -38.40 -23.25
39 1.80 -7.12 -9.58 -2.34 28.00 -43.25 -43.20 -28.25
40 2.00 -7.30 -9.62 -2.29 30.00 -45.82 -45.78 -30.89
41 2.40 -7.67 -9.67 -2.16 34.00 -48.87 -48.84 -34.00
42 2.80 -8.21 -9.83 -2.02 37.00 -50.53 -50.51 -35.70
43 3.00 -8.52 -9.94 -1.94 40.00 -51.69 -51.67 -36.88
44 3.40 -9.13 -10.17 -1.76 45.00 -61.36 -61.35 -46.61
45 3.70 -9.66 -10.41 -1.61 50.00 -56.03 -56.03 -41.34
46 4.00 -10.23 -10.72 -1.47 55.00 -65.17 -65.17 -50.45
47 4.50 -11.19 -11.30 -1.21 60.00 -64.24 -64.23 -49.50
48 5.00 -12.21 -12.00 -0.92 65.00 -45.22 -45.21 -30.47
49 5.50 -13.20 -12.75 -0.61 70.00 -50.08 -50.09 -35.41
50 6.00 -14.18 -13.58 -0.34 75.00 -54.71 -54.69 -39.92
51 6.50 -15.13 -14.43 -0.11 80.00 -51.77 -51.75 -36.94
52 7.00 -16.15 -15.39 0.00 90.00 -38.60 -38.70 -24.43
53
54 'E' Exit ; 'R' Resonance Comp ; 'N' New File
55 'I' Increment DR , 'T' - Computer Adjustment
56 'C' Continue lower DR , 'S' - change RESET
57

```

FIGURE 11-1

Adjustment of Loop Gain -
 Ch # 1

OL amp Open Loop } Test
 CL amp Closed Loop } Data
 WRC Closed Loop with Res. Comp.
 Amplitude Ratio db vs Frequency
 CL amp adjusted for Mp=0 db above 1.0 hz
 WRC amp adjusted for Mp=0 db at 1.0 hz

```

in TRY
Bandwidth ?
4.0
try for 4.00 Hz bandwidth

Peak at 5.50 Hz ; delta_gain = 10.52 db for Mp= 0 db
RF= 35.00, DR= 2.00, Peak f= 5.50 Hz

Peak at 5.00 Hz ; delta_gain = 10.15 db for Mp= 0 db
RF= 25.00, DR= 2.00, Peak f= 5.00 Hz

Peak at 4.50 Hz ; delta_gain = 9.97 db for Mp= 0 db
RF= 20.00, DR= 2.00, Peak f= 4.50 Hz

Max LF DEV = -3.65 db: -1 db BW= 5.00 Hz ; -20db at 10.00 Hz
data file being analyzed - pl-trial.dat;

FREQ : OL amp: CL amp  WRC : FREQ : OL amp: CL amp  WRC
0.10  2.88  0.51  0.91   7.00 -15.39  0.00  -7.49
0.15  1.32  0.66  1.13   7.50 -16.36 -0.02  -9.46
0.20 -3.12  0.16  0.13   8.00 -17.35 -0.36 -11.31
0.30 -6.95 -1.00 -1.80   9.00 -19.28 -1.69 -14.59
0.40 -8.66 -1.83 -3.01  10.00 -21.08 -3.50 -17.46
0.60 -9.29 -2.34 -3.65  12.00 -23.30 -5.95 -21.32
0.80 -9.32 -2.37 -3.63  14.00 -26.30 -9.60 -25.63
1.00 -9.40 -2.41 -3.62  16.00 -28.72 -12.49 -29.16
1.20 -9.43 -2.40 -3.56  18.00 -31.04 -15.18 -32.44
1.40 -9.53 -2.41 -3.50  20.00 -33.59 -18.05 -35.86
1.60 -9.56 -2.38 -3.38  24.00 -38.40 -23.25 -42.22
1.80 -9.58 -2.34 -3.24  28.00 -43.20 -28.25 -48.39
2.00 -9.62 -2.29 -3.06  30.00 -45.78 -30.89 -51.61
2.40 -9.67 -2.16 -2.62  34.00 -48.84 -34.00 -55.88
2.80 -9.83 -2.02 -2.11  37.00 -50.51 -35.70 -58.40
3.00 -9.94 -1.94 -1.84  40.00 -51.67 -36.88 -60.36
3.40 -10.17 -1.76 -1.22  45.00 -61.35 -46.61 -71.28
3.70 -10.41 -1.61 -0.75  50.00 -56.03 -41.34 -67.12
4.00 -10.72 -1.47 -0.36  55.00 -65.17 -50.45 -77.36
4.50 -11.30 -1.21  0.00  60.00 -64.23 -49.50 -77.45
5.00 -12.00 -0.92 -0.39  65.00 -45.21 -30.47 -59.41
5.50 -12.75 -0.61 -1.59  70.00 -50.09 -35.41 -65.20
6.00 -13.58 -0.34 -3.41  75.00 -54.69 -39.92 -70.72
6.50 -14.43 -0.11 -5.40  80.00 -51.75 -36.94 -68.63
7.00 -15.39  0.00 -7.49  90.00 -38.70 -24.43 -57.06
  
```

FIGURE 11-2

Adjustment of Loop Gain
 & Resonance Compensation
 Ch# 1

```

1 Remove RESET - type '1', RPM = 20
2 Add RESET - type '2', RPM = 20
3 Change Resaet - type '3' RPM = 20
4
5 3 600
6 Break Freq = 0.159
7 Break Freq = 1.592
8
9 Peak at 7.00 Hz ; delta_gain = 14.71 db for Mp= 0 db
10 Max LF DEV = -2.41 db; -1 db BW= 8.00 Hz ; -20db at 20.00 Hz
11 closed loop adjusted for Mp=0 db , rpm = 600
12
13 data File being analyzed - pl-trial.dat with Reset = 600 RPM
14
15 FREQ OL amp: OL ph Oamp: FREQ OL amp: OL ph Oamp
16 0.10 8.24 -145.01 0.51 7.00 -16.15 -126.17 0.00
17 0.15 2.09 -124.00 0.66 7.50 -17.14 -131.31 -0.02
18 0.20 -1.85 -101.24 0.16 8.00 -18.11 -135.34 -0.36
19 0.30 -4.95 -76.49 -1.00 9.00 -19.97 -141.90 -1.69
20 0.40 -6.32 -60.11 -1.83 10.00 -21.69 -147.25 -3.50
21 0.60 -6.43 -43.07 -2.34 12.00 -23.82 -156.20 -5.95
22 0.80 -6.44 -41.53 -2.37 14.00 -26.70 -165.46 -9.60
23 1.00 -6.56 -41.50 -2.41 16.00 -29.03 -172.78 -12.49
24 1.20 -6.63 -42.36 -2.40 18.00 -31.28 -180.74 -15.18
25 1.40 -6.84 -44.37 -2.41 20.00 -33.77 -186.36 -18.05
26 1.60 -6.98 -46.86 -2.38 24.00 -38.50 -199.84 -23.25
27 1.80 -7.12 -49.66 -2.34 28.00 -43.25 -205.94 -28.25
28 2.00 -7.30 -52.92 -2.29 30.00 -45.82 -200.99 -30.89
29 2.40 -7.67 -60.02 -2.16 34.00 -48.87 -204.40 -34.00
30 2.80 -8.21 -67.26 -2.02 37.00 -50.53 -208.55 -35.70
31 3.00 -8.52 -70.81 -1.94 40.00 -51.69 -217.76 -36.88
32 3.40 -9.13 -77.79 -1.76 45.00 -61.36 -191.05 -46.61
33 3.70 -9.66 -83.03 -1.61 50.00 -56.03 -278.25 -41.34
34 4.00 -10.23 -87.80 -1.47 55.00 -65.17 -224.60 -50.45
35 4.50 -11.19 -95.40 -1.21 60.00 -64.24 -195.16 -49.50
36 5.00 -12.21 -102.54 -0.92 65.00 -45.22 -100.36 -30.47
37 5.50 -13.20 -109.32 -0.61 70.00 -50.08 -283.39 -35.41
38 6.00 -14.18 -115.29 -0.34 75.00 -54.71 -169.55 -39.92
39 6.50 -15.13 -120.83 -0.11 80.00 -51.77 -179.15 -36.94
40 7.00 -16.15 -126.17 0.00 90.00 -38.60 8.63 -24.43
41
42
43 'E' Exit ; 'R' Resonance Comp ; 'N' New File
44 'I' Increment DR , 'T' - Computer Adjustment
45 'C' Continue lower DR , 'S' - change ReSet
46 'G' Add Integral Compensation

```

FIGURE 11-3

Type 3 - Change Reset
from 60 rpm to 600 rpm

OL amp - Open Loop } RPM = 600
CL amp - Closed Loop }
Oamp - Closed Loop adjusted for Mp=0 db above 1.0 hz
Amplitude Ratio db vs Frequency

```

47 First Break Freq in Hz ?? , Second Break Freq ??
48 .1 1.
49 Integral Compensation from 0.10 Hz to 1.00 Hz
50 Peak at 2.80 Hz ; delta_gain = 24.43 db for Mp= 0 db
51
52 data File being analyzed - p2-try5.dat with Reset = 20 RPM
53
54 FREQ ,IC(OL-Ph: db OL CL) ; FREQ ,IC(OL-PH: db OL CL)
55 0.05 -159.05 16.19 0.08 6.00 -128.71 -28.03 -1.45
56 0.10 -146.53 5.27 0.24 6.50 -131.83 -28.98 -2.03
57 0.20 -96.63 -3.12 0.05 7.00 -134.94 -29.87 -2.69
58 0.25 -87.62 -3.75 -0.07 7.50 -138.04 -30.73 -3.41
59 0.30 -84.63 -4.63 -0.13 8.00 -141.04 -31.64 -4.30
60 0.40 -82.92 -5.78 -0.18 9.00 -146.40 -33.27 -6.07
61 0.50 -86.02 -7.16 -0.16 10.00 -150.72 -34.99 -8.12
62 0.60 -86.84 -8.13 -0.17 12.00 -159.94 -36.61 -9.95
63 0.80 -89.45 -10.54 -0.19 14.00 -168.83 -39.19 -13.05
64 0.90 -90.73 -11.47 -0.19 16.00 -176.28 -41.52 -15.78
65 1.00 -91.61 -12.15 -0.19 18.00 -183.49 -43.56 -18.11
66 1.20 -93.76 -13.53 -0.19 20.00 -190.29 -45.53 -20.31
67 1.40 -96.11 -14.67 -0.16 24.00 -204.47 -49.35 -24.46
68 1.60 -98.70 -15.70 -0.10 28.00 -217.59 -53.71 -29.04
69 1.80 -100.28 -16.60 -0.09 30.00 -221.34 -56.35 -31.75
70 2.00 -101.97 -17.44 -0.06 34.00 -227.81 -60.89 -36.37
71 2.40 -105.32 -18.93 -0.01 37.00 -233.85 -64.73 -40.25
72 2.80 -108.07 -20.29 -0.00 40.00 -260.42 -69.94 -45.50
73 3.00 -109.35 -20.91 -0.01 45.00 -196.46 -67.03 -42.54
74 3.40 -112.12 -22.09 -0.03 50.00 -224.30 -76.23 -51.78
75 3.70 -114.01 -22.87 -0.08 55.00 57.32 -70.41 -46.00
76 4.00 -116.05 -23.61 -0.12 60.00 -113.87 -61.99 -37.51
77 4.50 -119.20 -24.86 -0.33 65.00 -72.78 -65.69 -41.28
78 5.00 -122.42 -26.00 -0.61 70.00 -137.92 -65.09 -40.59
79 5.50 -125.62 -27.06 -0.98 75.00 -162.00 -62.70 -38.16
80 6.00 -128.71 -28.03 -1.45 80.00 -199.52 -58.02 -33.42
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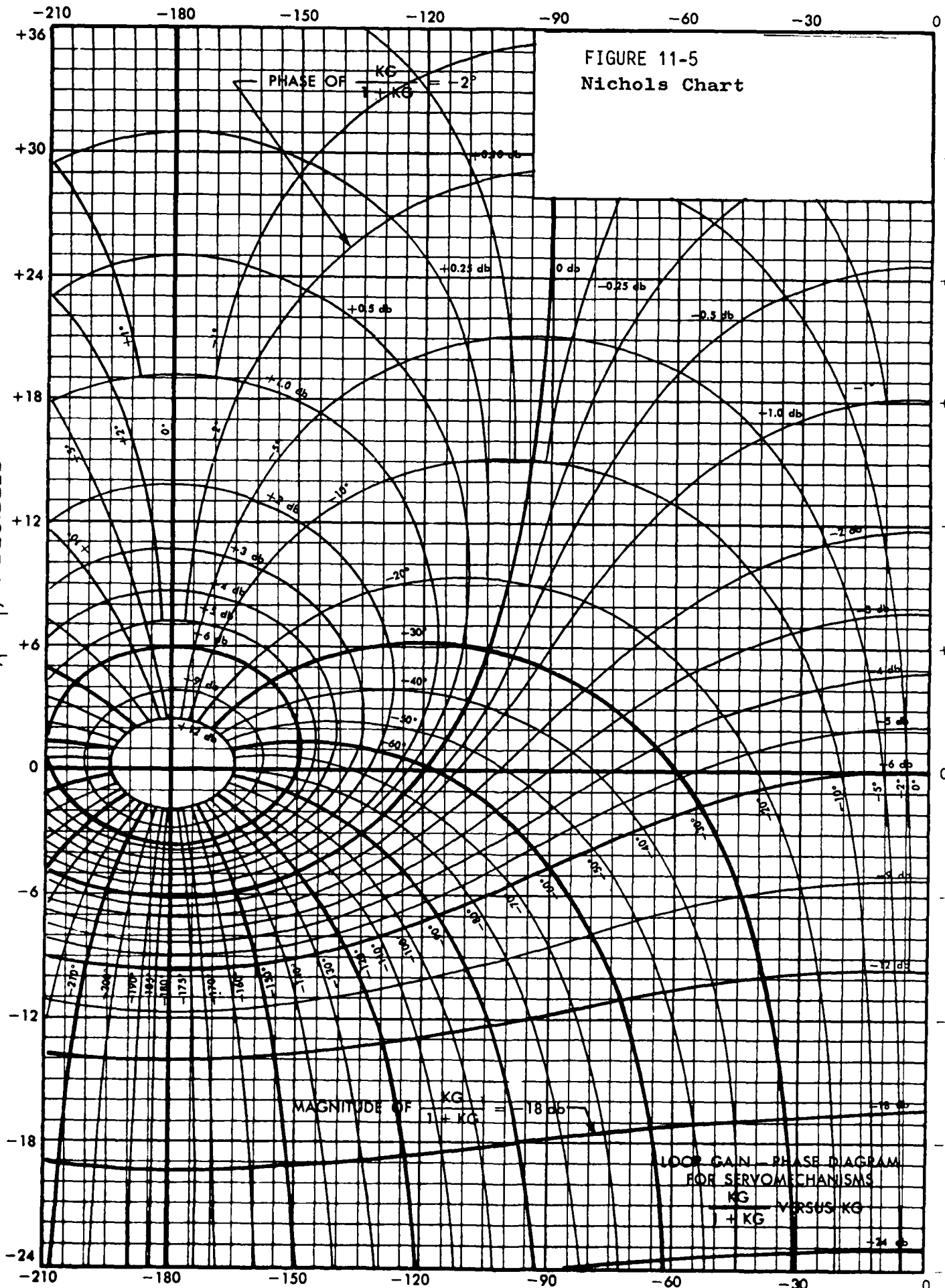
FIGURE 11-4

OL-Ph Open Loop Phase
db-OL Open Loop Gain
db-CL Closed Loop Gain

Reset Changed to 20 RPM
Integral Compensation Added
0.1 hz 1.0 hz Break Frequencies

OPEN - LOOP GAIN, $|KG|$, IN DECIBELS

FIGURE 11-5
Nichols Chart



OPEN-LOOP PHASE, $\angle (KG)$, IN DEGREES
120

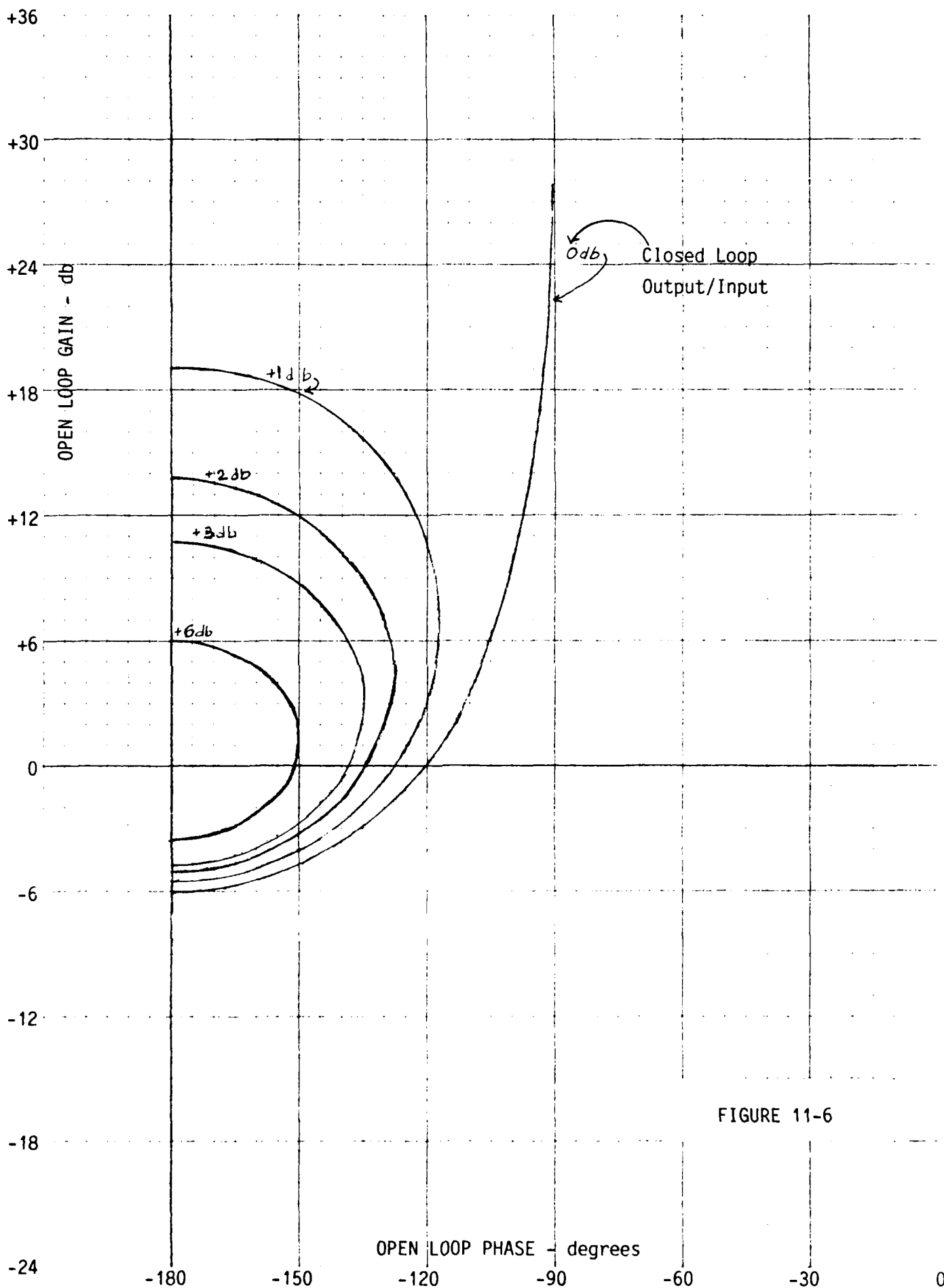


FIGURE 11-6

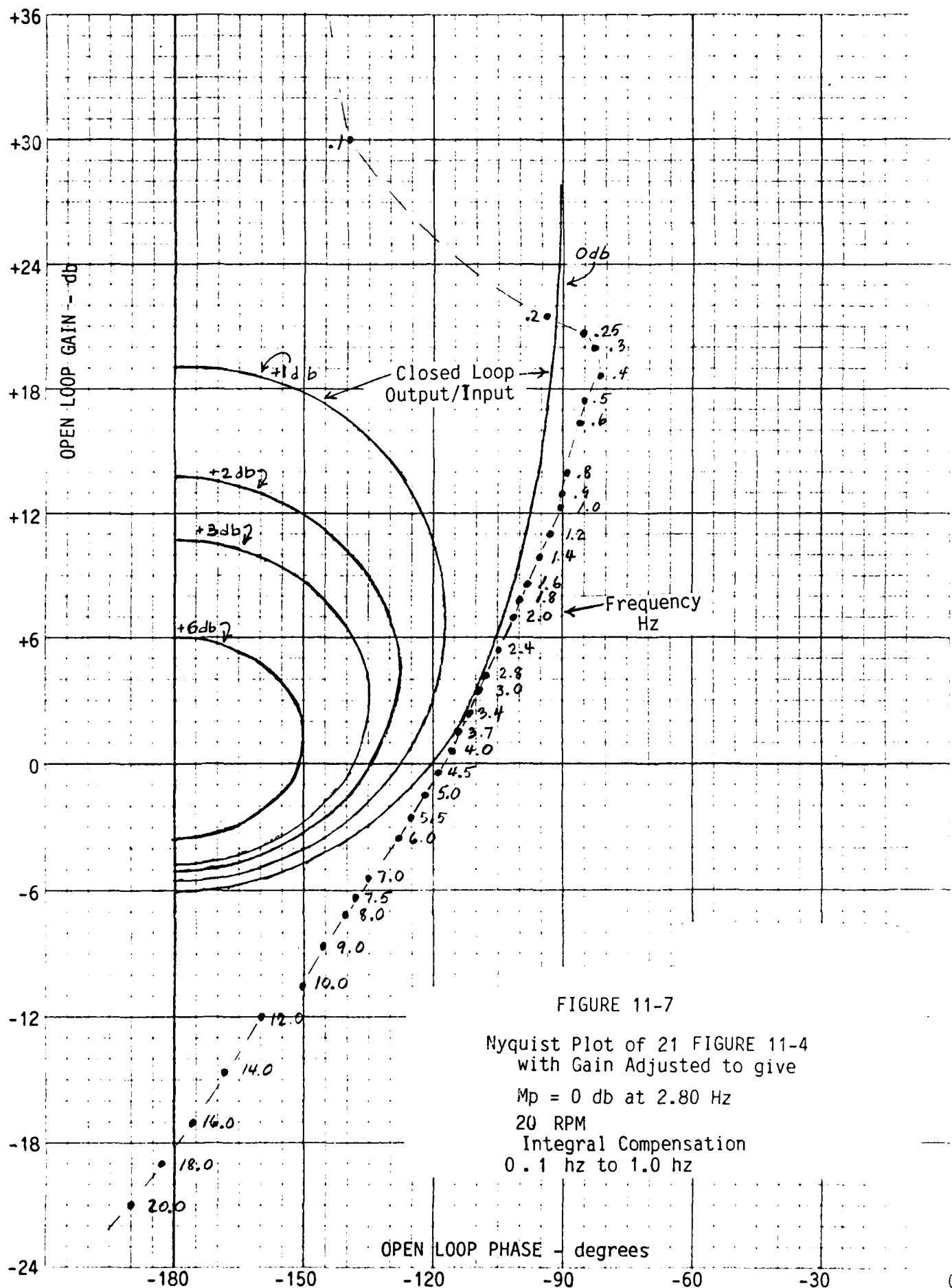


FIGURE 11-7

Nyquist Plot of 21 FIGURE 11-4
with Gain Adjusted to give

$M_p = 0$ db at 2.80 Hz

20 RPM

Integral Compensation

0.1 hz to 1.0 hz

```

1 0 7 4 2
2 50.0 2.0 100. 6
3 1 3 5 4
4 50.0 2.0 100. 6
5 2 0 0 0
6
7 /*organization of the WPAFB test setup -
8 system number - Controller - RC - Channel -
9 RC freq, RE_dr, Cont_pb, Cont_rpm -
10 */
11 B>

```

FIGURE 12-1

'SETUP.DAT' file
for use by 'RCO'.

Permits 'RCO' to read
system organization and
recommended settings.

System '0' and System '1' are in use.

System '2' is not in use.

Computer OPERATOR

"NUMBER of SYSTEMS in USE 1,2,3 ? "
"NUMBER of SYSTEMS = 2 "

"READING FROM DISC ARE:"
"System 1, Controller 7, RC4, Channel 2 "
"Read as RF = 50.0 : DR = 2.0 : PB = 100 : RPM = 6 "

"System 2, Controller 3, RC 5, Channel 4 "
"Read as RF = 50.0 : DR = 2.0 : PB = 100 : RPM = 6 "

"ENTER PROVEN SETTINGS INTO SYSTEM 1,2,3 ? OR NO MORE 0" 2
"SYSTEM 2 SET to RF = 50.0 Hz DR = 2.0 PB = 100.0 Reset = 6 OFF" 1
"SYSTEM 1 SET to RF = 50.0 Hz DR = 2.0 PB = 100.0 Reset = 6 OFF" 0

"SETTINGS COMPLETED"
"manual change Resonance Compensation - 'R'"
"manual change PB-'B' RESET (rpm) - 'M'"
"exit - 'E' : Display Present Values - 'D'"
"RESET - ON - OFF 'S'"

(menu)

"SYSTEM # - pb - 1.0 to 100.0% ??"
"SYSTEM # 1 to have 45.0 PB" b B
1 45.0

"SYSTEM #, RESET RPM 6 to 6000 : ON '1' OFF '0' ??" m M
1 35 0

"SYSTEM #, Break Frequency, Damping Ratio ??" r R
2 25.0 1.75

"SYSTEM #2 to have, Break Frequency = 25.0, Damping = 1.75" s S
1
0

"SYSTEM # '1','2','3' ? Finished 0"
"System #1 has RESET 35 rpm with RESET OFF"
"RESET ON - '1' : RESET OFF - '0' ?"
"SYSTEM # '1','2','3' ? Finished 0" d D
1
0

"SYSTEM #1 uses CONT # 7, RC # 4, CHANNEL # 2"
"CONTROLLER set at 45.0 PB, 35 rpm and is ON"
"RC-set at 50.0 Hz, and at 2.0 DR"

"SYSTEM #2 uses CONT # 3, RC # 5, CHANNEL # 4"
"CONTROLLER set at 100.0 PB, 6 rpm and is OFF"
"RC set at 25.0 Hz, and at 1.75 DR"

b B
1 45.0
m M
1 35 0
r R
2 25.0 1.75
s S
1
0
d D

h or H - menu repeats
e or E - exit from program

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES	
APPROVALS	DATE		
CHECKED			
SCALE		SIZE	
DO NOT SCALE DRAWING		FIGURE 12-2	
SHEET			

DRF, INC.

COMPUTER PROGRAM OF
CONTROL PARAMETERS

'RCO'

Program to Computer set Controllers & Resonance Compensation
Boards in up to three systems

REVISIONS		
DESCRIPTION	DATE	APPROVED

Figure 12-2. 'RCO' - Computer Program of Control Parameters